Simulating the Impact of Poly-CD Wafer-Level and Die-Level Variation On Circuit Performance

Brian E. Stine, Duane S. Boning, James E. Chung, *Dennis Ciplickas, *John K. Kibarian
MIT EECS, Cambridge MA 02139, *PDF Solutions, San Jose, CA 95110

ABSTRACT

In this paper, we present a methodology for simulating the impact of wafer-level (within-wafer) and die-level (within-die) variation on circuit performance. For a sample 0.25μm 64x8 SRAM layout, the impact of both die-level and wafer-level poly-CD variation as measured through signal skew and delay is shown to be significant.

INTRODUCTION

The design of high speed integrated circuits must account for device and interconnect variation within the circuit. Traditionally, this has been accomplished by way of design rules, which govern the shape and proximity of various layout structures, and worst-case/best-case device model (SPICE) files. For analog circuitry, careful attention to device matching within the circuit is required, while digital designers have proceeded comfortable in the belief that variation within the circuit will be small and will not disturb digital operation. As clock speeds have risen, however, the importance of device and interconnect variation in limiting performance has increased. Furthermore, the relative magnitude of manufacturing variation is increasing. To continue technology and circuit performance improvements, manufacturing variation and its impact on high performance VLSI circuits must be better understood.

Especially important is variation in the polysilicon critical dimension, or poly CD, which translates directly into MOS transistor channel length variation and resulting variations in the drive current and switching characteristics. Current lithography and etch technology can typically achieve wafer-scale line width uniformity of approximately +/- 5-10% (measurements of the same structure within each chip across the wafer). Design rules typically assume that the variation within any one chip will be smaller than this value. However, measurements of supposedly identical structures within the same die reveal variations on the order of 15-20% [1]. Clearly, additional physical effects are coming into play at this scale, such as pattern dependencies during etch or systematic lens distortions during photolithography.

Spatial variation usually consists of wafer-level (or within-wafer) variation and die-level (or within-die) variation as well as other systematic components. As shown in Figure 1, statistical and signal processing methods can be used to discriminate these scales of variation to achieve decomposition [2, 3]. Previous studies have empirically observed a correlation between poly-CD variation and circuit performance (e.g. [4]) for small circuits (such as ring-oscillators), but predictive modeling of the impact of die-level and wafer-level variation has been difficult. In this paper, we develop a methodology for simulating the impact of poly-CD die-level variation and wafer-level variation on circuit performance.

SIMULATION METHODOLOGY

We propose the methodology shown in Figure 2 for exploring the impact of wafer-level and die-level variation on circuit performance. The methodology uses aerial imaging simulation (e.g. [5]) to predict the expected die-level poly-CD variation for a given layout. Aerial imaging incorporates optical projection physics and may include simple etch models to predict the expected poly-CD variation at all points on a layout. For the aerial imaging simulator we used, a light source of 248nm and a coherence value of 0.5 was used with a lens numerical aperture (NA) of 0.5. Lens aberrations and resist development/coating effects were not incorporated in our simulator due to lack of this information. After aerial imaging, the netlist is extracted from the modified layout.

The wafer-level variation is simulated by biasing every channel length parameter in the netlist up or down depending on the particular location on the wafer. Inherent in this step is the assumption that within a die, the wafer-level variation is nearly constant and thus represents only a shift in the mean of the population of the aerially imaged and extracted channel lengths. Finally, the biased netlist is simulated using SPICE and suitable performance metrics are extracted. A loop is wrapped around the biasing and SPICE simulating steps to gather data for compact modeling the performance metrics as a function of mean channel length. Typically, critical delay, i.e. the delay of the slowest path in the circuit, is extracted as a measure of the impact of wafer-level variation, and skew, i.e. the spread in delay across all output ports, is extracted as a measure of the impact of die-level variation. As we will see, it is also possible for these effects to couple so that the amount of skew is dependent not only on the spread and nature of the distribution of poly-CD variation, but also on its mean value.

SIMULATION EXAMPLE

A 64x8 SRAM macrocell was chosen to illustrate the simulation methodology described in the previous section. The layout is approximately 180μm x 140μm in size and contains approximately 4000 transistors. The layout was originally designed for 3μm design rules but was scaled down to 0.25μm design rules.

The hypothetical wafer-level variation is shown in Figure 4. A “bull’s eye” pattern has been assumed and is empiri-

cally consistent with the data presented in [6]. “Bull’s eye” effects are commonly seen for wafer-level variation due to wafer-scale macroloading during etch [7]. A +/- 5% variation in channel length is assumed across an 8” wafer.The result of simulating the layout in Figure 3 with an aerial imaging simulator is shown in Figure 5. Significant die-level variation in poly-CD variation can be seen across the entire cell of approximately +/- 10%.

For the SPICE simulations, a 0.25µm device model was created based on SIA roadmap specifications [8, 9] and typical values reported in the literature. The sensitivity of Id_{SAT}, the measured drain current, when both the gate and drain are held at the supply rail, is shown in Figure 6. Although the Id_{SAT} values are slightly higher than normally expected, the sensitivity to channel length variation is similar to results published elsewhere (e.g. [10]).

DISCUSSION

Figure 7 shows a simple SPICE simulation output for the mean channel length biased near 0.25µm (i.e. assuming the wafer-level variation is near zero). Note that only devices were extracted from the aerially imaged layout and that interconnect capacitance was only crudely estimated by the addition of identical load capacitances at all outputs. For this study, two SRAM performance parameters were simulated: (1) the write access time or write cycle delay and (2) the read access time or read cycle delay. The write access time is the delay time required for an input word to store. The read access time is the delay between the assertion of an address line and the output of the stored word. As Figure 7 shows, there is considerable skew for the write cycle but very little skew for the read cycle. This is in sharp contrast to simulations of non-aerially imaged layouts which show virtually no skew for either cycle.

A model of read cycle and write cycle delay and skew versus mean channel length is shown in Figure 8(a,b). A strong linear trend is observed. Note that the write cycle skew is strongly correlated to the mean channel length compared to an extremely weak dependence for the read cycle skew. The write cycle skew corresponds to over 60% of the total write cycle delay. The dependence of delay and skew on load capacitance is shown in Figure 8c. As the load capacitance increases the total delay also increases but the skew remains relatively constant indicating that as the load capacitance increases the ratio of skew to delay decreases. Thus, the impact of wafer-level variation on circuit performance may be greater than die-level effects for large capacitive loads. This effect, however, may also be modulated by any interconnect variation and cautious interpretation is needed.

Figure 9 shows the estimated wafer-maps of the skew and delay versus spatial position. Both skew and delay are strongly dependent on spatial position and resemble the wafer-level variation as expected from the linear nature of the dependence of skew and delay on channel length and as reported in [4]. The correlation between skew and spatial position (or the wafer-level variation) is especially problematic since it suggests that the effect of die-level variation on circuit performance is correlated with wafer-level variation as well. In addition, wafer-die interaction and residual terms (see Figure 1) may also contribute to the vexing nature of the problem. The results shown in Figures 8 and 9 also indicate that the ratio of skew to delay across the entire wafer is nearly constant at 63% for a fixed load capacitance of 10fF.

CONCLUSION

In this paper, we have presented a methodology for simulating the effect of both wafer-level and die-level poly-CD variation on circuit performance. Both wafer-level and die-level poly-CD variation impact the circuit performance for an example 0.25µm 64x8 SRAM layout and hypothetical wafer-level variation. Wafer-level variation and die-level variation induced performance effects can couple.

Further study is needed to identify the impact of interconnect die-level and wafer-level variation as well as poly-CD variation. Also, the continued development of wafer-level and die-level predictive and calibratable models is necessary for the accurate determination and modeling of the impact of spatial/pattern dependent variation on circuit performance. We are also interested in the interrelationships between scaling, circuit performance, and wafer- and die-level variation. Finally, the methodology and results need to be compared with end-of-line E-test measurements for calibration and validation.

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