Failure Mode Detection and Process Optimization for 65 nm CMOS Technology

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Abstract – Short loop test flows have been commonly used in back end of line (BEOL) interconnect process development to speed up learning rates and improve yields. This paper presents case studies on the expanded use of short loop test chips to the Shallow Trench Isolation (STI), Gate and Pre-Metal Dielectric (PMD)/Contact loops of a 65nm process technology in addition to the BEOL. These test chips have been used to quickly identify and eliminate random and systematic defect mechanisms and generate a robust process flow, thus accelerating the rate of yield learning.

INTRODUCTION

Die size and ramp to yield entitlement are the key components of success for any CMOS technology. Once a competitive set of design rules is selected and an initial integration process developed, the ramp rate to volume yield entitlement is the most important metric for success and profitability. During early development systematic fail mechanisms usually dominate the yield pareto, while by the end of the ramp to volume production, entitlement is limited by random defect fail mechanisms. Traditionally, the initial systematic failure mechanisms are detected and eliminated using a combination of passive parametric structures and a SRAM yield test die, followed by initial product prototype production. Final entitlement is then achieved using a high volume product. Using this methodology, the learning rate is limited by amount of material processed and cycle time of full flow SRAM or production material. Prioritizing key lots to reduce learning cycle time can only decrease the overall learning cycle time to the extent a factory can process full flow material.

To further accelerate learning, short flow test dies with a reduced number of mask levels can be leveraged to reduce defectivity in specific process loops more rapidly than with full flow material. Dedicated short flow test die in the shallow trench isolation (STI)/Gate loop, pre-metal dielectric (PMD)/Contact loop, and back end of line (BEOL) allow learning in three areas of the flow simultaneously. Results of each of these short loops can then be incorporated on the next learning cycle of full flow material for an overall acceleration of learning verses learning strictly on full flow material.

EXPANDED USE OF SHORT FLOW TEST DIE TO ACCELERATE RAMP TO YIELD ENTITLEMENT

Yield management and analysis tools [1-4] require accurate defect density information for yield prediction tools to make accurate yield predictions. Defect density (DD) test die consisting of passive parametric structures are one method to generate accurate defect density data of electrical killer defects. SRAM and other addressable arrays [5,6] can give

similar information but require more mask levels than passive structures. While dedicated BEOL DD test die have been used for several generation to generate this information and drive BEOL yield learning, short flow devices in the front end of the line (FEOL) and the PMD/Contact loops have generally consisted of limited structures for basic transistor/isolation integration and process development. The limited coverage of these structures makes them unsuitable as inputs for yield analysis tools and as yield drivers in these loops.

At the 65 nm node, the DD test die methodology of the BEOL short flow device was expanded to the STI/Gate loop, and the PMD/Contact loop. The addition of these test die give process loop teams working in these areas a new quantifiable metric to judge the impact of proposed process improvements on electrical fail rates. By combing the DD information from the short flows with critical area analysis (CAA) and other yield management tools, yield predictions based on DD test die electrical failure rates can be calculated.

Expanding the use of short flows can accelerate DD learning in two ways versus full flow material. First, the mask count of the short flows greatly reduces the feedback loop between lot start and electrical results. For example, a typical 65 nm full flow device can have 28 or more mask levels, while short flows for various loops can yield valuable information with between 2 and 6 mask levels. The second way short flows accelerate learning is the simplicity of structures and ease of detecting and isolating failures. Typical comb/serpent structure and via/contact chains are small enough that hard opens and shorts can easily be isolated using the typical PFA methodologies.

DESCRIPTION OF SHORT FLOW TEST DIE

STI/Gate Loop Test Dies

For the STI/Gate loop, a two mask test die (Active and Poly) was used. The test modules consist of Polysilicon comb/serpent structures with and without underlying Active topography. Design of Experiments (DOE's) explore the full design rule space through pitch. For STI fill and Gate loop defectivity learning, the short flow can be set up with a limited number of implants for quickest possible cycle time. For implant damage learning, an expanded set of implant steps can be incorporated into the process flow. After processing through the silicide loop, testing can be done directly on silicided bond pads. Since no PMD or protective

oxide (PO) is present, isolation of electrical fails becomes quite straightforward.

Contact loop Test Die

The Contact short flow is a six mask test die (Active/Poly/CT/MET1/PO/AlCAP) with a full set of Active and Poly comb/serpents, Active and Poly Contact chains, PMD and Tungsten CMP monitors, and Metal One comb/serpents and nested serpents. Both defect density structures and structures with DOE's to exercise potential systematic failure mechanisms are included. Figure 1 compares a comb/serpent with a nested serpent structure [7]. Nested serpent structures have proven useful in determining the size distribution of defects that cause electrical fails. By compiling the number of metal leads that are shorted or open at each fail location in the nested serpents, a size distribution of defects which cause electrical fails can be determined and compared to the size distribution of defects found by traditional YE techniques to better understand which defects detected in-line at YE turn into electrical failures.

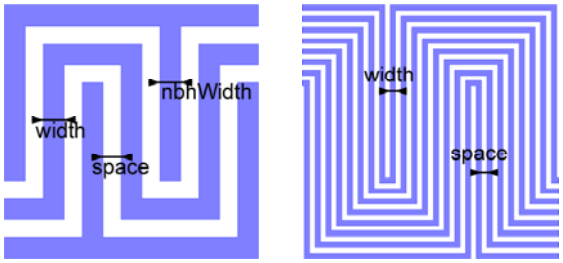

Figure 1. Schematic of Snake/Comb and "Nest" structures

ACCELERATED LEARNING WITH SHORT FLOW TEST DIE

Results from short flow test die (STI loop)

In the case of the STI loop, initial electrical results showed heavy Poly shorting at the edge of the wafer when Poly comb/serpents ran over minimum space Active features (Figure 2). The fail rate dropped two orders of magnitude over non-minimum geometry Active features (Figure 3), so a minimum geometry STI fill issue was suspected.

Failure analysis (Figure 4) verified that STI voids were the root cause of Poly shorts. Once the problem was identified, the short flow test die was used as a quantitative metric to validate process improvements. Figure 5 shows the Poly shorts fail rate improvement with each learning cycle. In the time necessary for one full flow learning cycle, five learning cycles of the short flow were completed and a robust process identified that could then be implemented on the first product of the technology with high confidence of success.

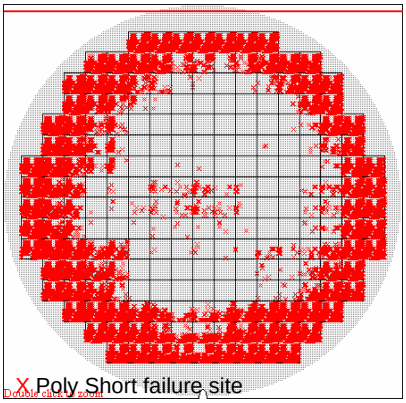

Figure 2. Fail site wafer map for Poly shorts.

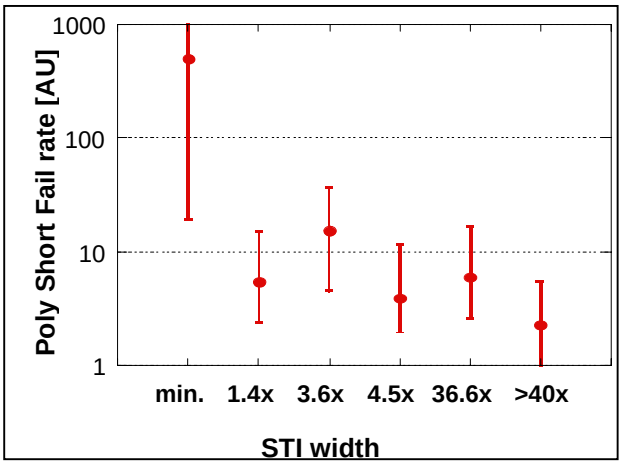

Figure 3. Poly short fail rate as a function of STI width.

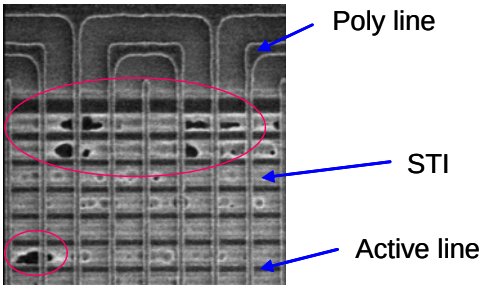

Figure 4. Top view of Poly short structures. Voids in STI can be found in the pink circles.

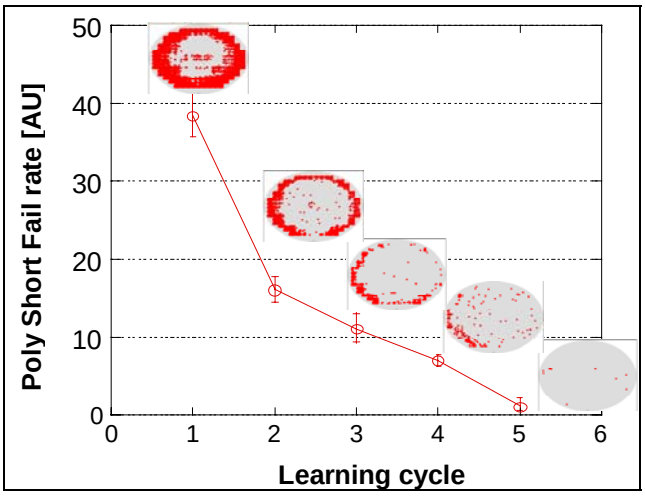

Figure 5. Reduction in Poly shorts over five process learning cycles. Red in the wafer yield maps represent failed dies.

Another advantage of the short loop STI loop die is learning on design rule clean features that may not be extensively used on the first product on the technology. For example, Figure 6 compares the instances of minimum space STI in the random logic of the 65 nm initial product vs. another early 65 nm prototype. The first product did not use minimum space STI features and the minimum space systematic shorting problem highlighted with the short flow DD test die may have gone undetected until it caused failures on the second prototype which made use of minimum space STI in random logic.

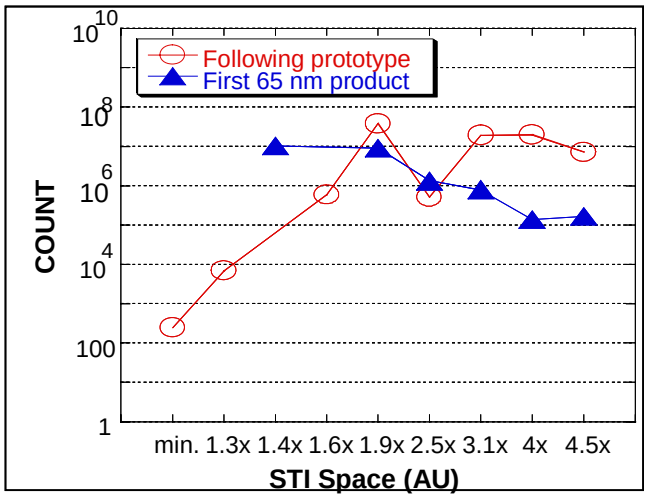

Figure 6. Comparison of the STI space use between the first 65 nm product (blue triangles) and a following prototype (red circles) in random logic. The first product did not fully exercise the random logic minimum space design rule.

Results from short flow test die (CT/PMD loop)

For the Contact loop, fail rates at 65nm geometries need to be in the low or sub ppb range for acceptable yields on large microprocessors and digital signal processors. While SRAM yield learning vehicles are often used to drive Contact learning, they can be less than optimal because layout sensitive fails that depress yields in random logic may go undetected. For example Figure 7 shows pitch dependent Contact yield variation from initial Contact short flow lots that the SRAM yield driver did not detect. Such isolated Contact fails would be quite difficult to isolate on a product with logic mapping and PFA.

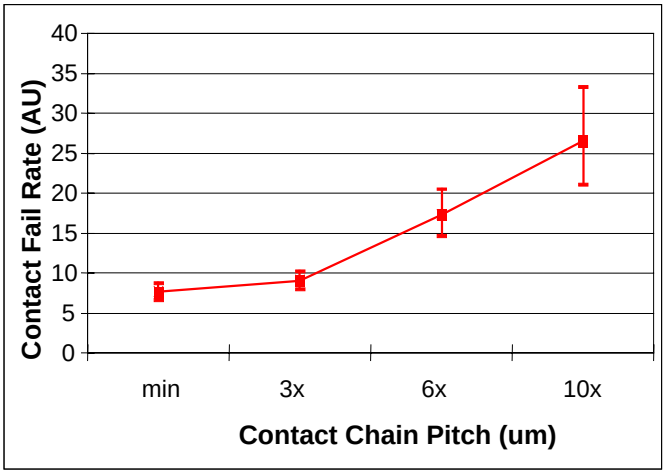

Figure 7. Increased fail rate of Contacts as a function of pitch.

The contact short loop test die was also a vehicle which quickly detected Contact loop induced Metal One shorts and allowed rapid learning to implement process fixes. Figure 8 compares Metal One fail rates with and without Contact processing and highlights the killer defects generated in the Contact loop. The nested Metal One serpents enable a particle size distribution of killer defects to be determined. The initial process had an unusual tail of large killer defects (Figure 9) which were determined to be PMD CMP rip outs filled with tungsten. Metal One shorts caused by tungsten CMP dishing over dense Contacts (Figure 10) was also highlighted. Process improvements using the short flow as a process improvement driver reduced the Metal One shorting fail rate over 60% in a single learning cycle without committing any full flow material (Figure 11).

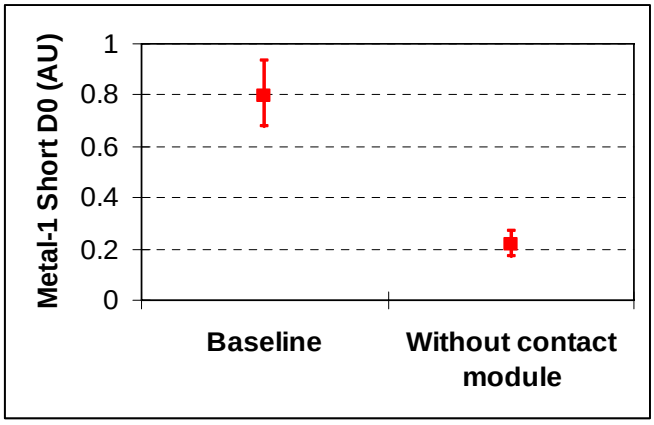

Figure 8. Comparison of Metal One short fail rate with and without Contact loop processing.

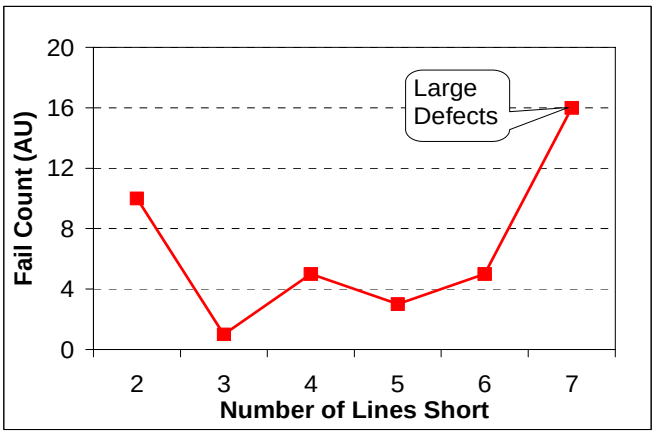

Figure 9. Metal One short defect size distribution by number of lines shorted.

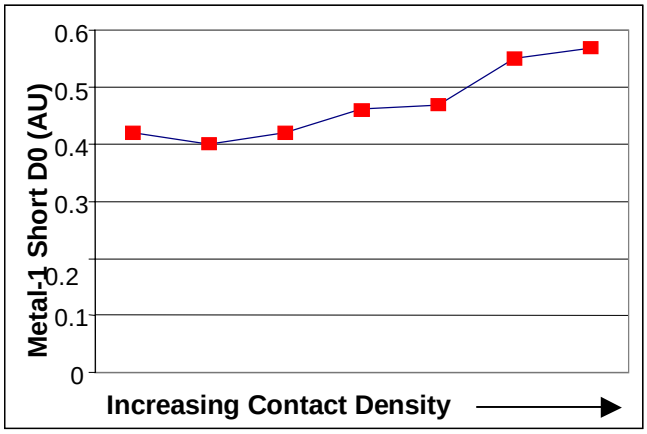

Figure 10. Metal One shorts increase as underlying Contact density increases.

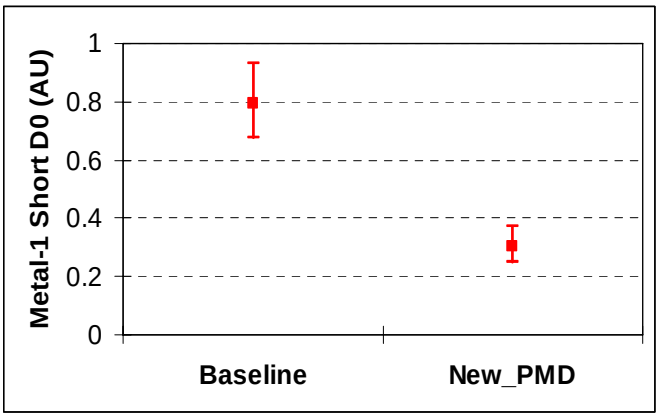

Figure 11. Comparison of Metal-1 short defectivity with "Old" and "New" PMD processes.

CONCLUSIONS

Increasing the ramp rate to entitlement is a major key to profitability in the semiconductor industry. Reducing cycle time of key full flow lots is one part of the solution. A second piece of the puzzle is to simultaneously learn on short flow test die dedicated for the various process loops in the flow with sufficient random DD and systematic test structures to quantify and eliminate failure mechanisms

By putting dedicated short flow DD test die in the hands of the process loop teams responsible for STI/Gate, and CT/PMD loop in addition to the BEOL teams, each of these teams can learn in parallel and process fixes from each area can be incorporated on full flow material for fastest possible ramp to yield entitlement.

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