Enabling Technology Scaling with "In Production" Lithography Processes

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ABSTRACT

As the industry hits a road block with RETs that attempt to aggressively scale k1, we propose to extend the life of optical lithography by a complete co–optimization between circuit choices, layout patterns and lithography. We demonstrate that the judicious selection of a small number of layout patterns along with the appropriate circuit topologies would not only enable k1 relaxation but also efficient implementation of circuits. Additionally, in this paper, we discuss the use of regular design fabrics to extend the life of current generation lithography equipment. We will introduce the Front End of Line (FEOL) limited regular design fabric. The metal 1 patterns for this fabric are selected such that we can utilize a 1.2 NA 32nm metal 1 lithography process without any area penalty with respect to standard cells with conventional design rules, which require a 32nm metal 1 process with a rather unrealistic k1 of 0.35 while using a more advanced 1.35 NA tool. We also demonstrate simulation results on 2-dimensional layout patterns. The results suggest that smart selection of layout patterns can enable the extension of single exposure lithography to a 32nm production lithography process.

Keywords: Regular design fabrics, FEOL limited fabric, bricks

1. NGL: NO GOOD LITHOGRAPHY SOLUTION

Optical lithography has been the work horse of the semiconductor industry for several generations that has enabled classical CMOS scaling by economically scaling the resolution, feature size and die area of integrated circuits (ICs) at every subsequent technology node. However, as the industry prepares for mass production of the 32nm technology node in 2010, the lack of an economically viable lithography solution has been at the forefront.

Historically, the wavelength (λ) of the light source as well as the numerical aperture (NA) was aggressively scaled to scale the minimum printable half – pitch by 70% at every subsequent technology node. More recently due the challenges associated with scaling the wavelength of the light source used for modern optical lithography systems the industry has moved from a regime of wavelength based resolution scaling to a k_1 based resolution scaling. In this regime, advancements in resolution enhancements techniques (RETs) have enabled the shrinking of k_1 and hence feature dimensions without changing the wavelength of the light source.

Although, the theoretical limit for k_1 is 0.25, values close to 0.4 are desired for single exposure lithography processes used in volume production of logic ICs The introduction of water immersion lithography has allowed for production lithography processes with k_1 higher than 0.4 for the 45nm technology node. However, at the 32nm technology node there is a lack of economically feasible lithography solutions that can operate at k_1 values below 0.4. The introduction of hyper – NA scanners with high index immersion liquids has been pushed to the 22nm technology node due to the unavailability of LuAG lens material with the desired level of transparency [2]. Even at the 22nm node, the challenges related to decreased throughput from the increased viscocity of high index fluids need to be solved. The introduction of EUV lithography would lead to an economically feasible production lithography process with k_1 significantly higher than 0.4. However, the challenges with the intensity of EUV light source, absorption of resist materials and mask manufacturing needs to be tackled before EUV can be considered for mass production of ICs [3]. Defectivity and throughput are primary concerns for the Nanoimprint Lithography (NIL) [4], especially for mass production of system on chips (SOCs). Maskless lithography solutions such as massively parallel E-beam writers offer a practical solution for low volume products. However, the significantly lower throughput makes is unattractive for mass production of ICs [5]. In the lack of technically feasible solutions to achieve resolution scaling, the industry is opting for multiple patterning strategies to meet the resolution requirements for the 32nm technology node [6]. Unfortunately, the decreased throughput and increased resist processing cost associated with multiple patterning solutions will lead to higher manufacturing costs at the 32nm node.

In order to have a cost-efficient 32nm technology node, the industry must find techniques of extending lithography tools techniques and processes already "in–production" to meet the goals for technology scaling. In this paper we propose a paradigm shift in IC technology development where resolution scaling is achieved by combined efforts of both the process and design communities. In Section 2 we discuss the evolutionary change and role of lithography as a circuit transfer technique for future technology nodes. Next, in Section 3, we discuss the task of limiting the total number of pattern in a design. We then give an overview of our proposed methodology for co-optimization between circuit topologies, layout patterns and lithography in Section 4. Finally, in Section 5, we discuss the lithography benefits of using regular design fabrics for 32nm technology node.

2. EVOLUTION OF IC DESIGN & MANUFACTURING

Lithography is, by definition, a pattern transfer technique. In the past a simple set of design rules was sufficient to ensure a What You See Is What You Get (WYSIWYG) paradigm and hence isolate both the design and manufacturing communities from the challenges faced by the other. As we keep pushing the limits of k_1 and operate production lithography processes close to values of 0.4 for k_1 it becomes increasingly difficult to resolve 2-dimensional patterns with sufficient image fidelity and process margins. Hence sub–100nm designs are often required to abide by several recommended design rules to account for failures that occur due to lithography, CMP, etch-loading, stresses in transistors and dielectrics, and other complex physical, chemical and mechanical interactions. In addition, the need for RET-compliant designs in more advanced process technologies has further increased the raw number and the complexity of these rules [7] and it has been the most significant contributor to the RTL to silicon design cost increase. In this regime where the layout patterns are severely constrained by lithographers to enable low k_1 processes, lithography can now be defined as a layout transfer technique. Unfortunately, the new expanded set of recommended design rules often leads to rules which are contradictory to the existing set of design rules and design goals. Consequently, designs that comply with these expanded set of design rules do not enable the 50% area shrink required for technology scaling thus undermining the number one objective for moving to the next node, namely the cost. Hence, to counter the challenges with achieving technology scaling, in this paper we propose to extend the single exposure optical lithography by conquering the final frontier – Design! In this regime lithographers must interact closer with the circuit and layout designers. By the judicious selection of circuit topologies, layout patterns and lithography choices simultaneously the process and design communities can work together to provide efficient and usable ICs. Thus lithography this would lead to the evolution of lithography to a circuit transfer technique.

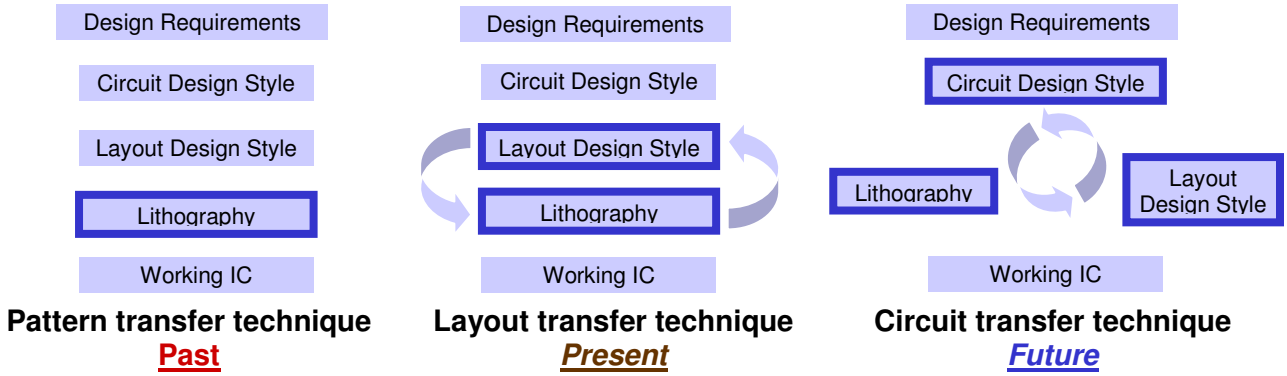


Figure 1: Role of lithography for past, present and future generations of IC design and manufacturing flows

3. LIMITING THE TOTAL NUMBER OF PATTERNS

Researchers have demonstrated application of source mask co-optimization (SMO) to maximize the lithographic process window for layout patterns used in circuits such as DRAMs [8] or SRAMs. The extremely predictable and limited set of layout patterns for memory circuits is the key enabler to such process layout co-optimization. The application of such techniques to random logic circuits that are designed using conventional design flows is far more difficult. It is observed that conventional application specific integrated circuits (ASICs) designed using standard cells based on simplistic design rules leads to designs with a large and unmanageable number of layout patterns. The huge size of the layout design space makes in impractical for lithographers to optimize lithography systems for all the possible layout patterns that could occur in the design. The need to optimize the resolution of lithography systems necessitates limiting the size of

the design space by limiting the total number of patterns. We propose the use of a regular design fabric to limit the total number of patterns in the design. However, it is observed that even with the extreme regularity imposed by regular design fabrics the total number of patterns in a design grows exponentially with the optical interaction length. Using a conservative optical interaction length of 2 – 6λ to define the size of a pattern leads again to an unmanageable number of patterns. It is known that optical region of influence of the pattern is a strong function of both the illumination conditions and also the perturbation introduced by the pattern. In the case of regular design fabrics, the layout patterns are minor perturbations from a grating. This perturbation is in the form of line–ends between two pieces of wire segments. In order to find a more accurate optical region of influence for 32nm patterns, we simulated the perturbation in the aerial image by introducing a line-end in a grating. Simulations were performed by rigorous simulations using EM–Suites from Panoramic Technologies. The simulation is performed for a standard 6% MoSi photomask, illuminated with cQuad source (0.85/0.65) using X-Y polarized light in a 1.35 NA immersion scanner. The perturbation due to a line–end introduced in the grating (Fig 2(c)) is computed by taking the difference between the aerial image in Fig 2(a) and Fig 2 (b). The outline in the solid black line drawn in Fig 2(c) bounds all regions where the change in aerial image intensity from the perturbation is greater than 5% of the imaging threshold. The dotted line shows the region of the layout that is 1 pitch away from the center of the line-end. Assuming an change of 5% of imaging threshold is significant to alter the lithographic properties of the pattern we can conclude that the optical region of influence spans slightly more than 1 pitch in either direction of the line – end.

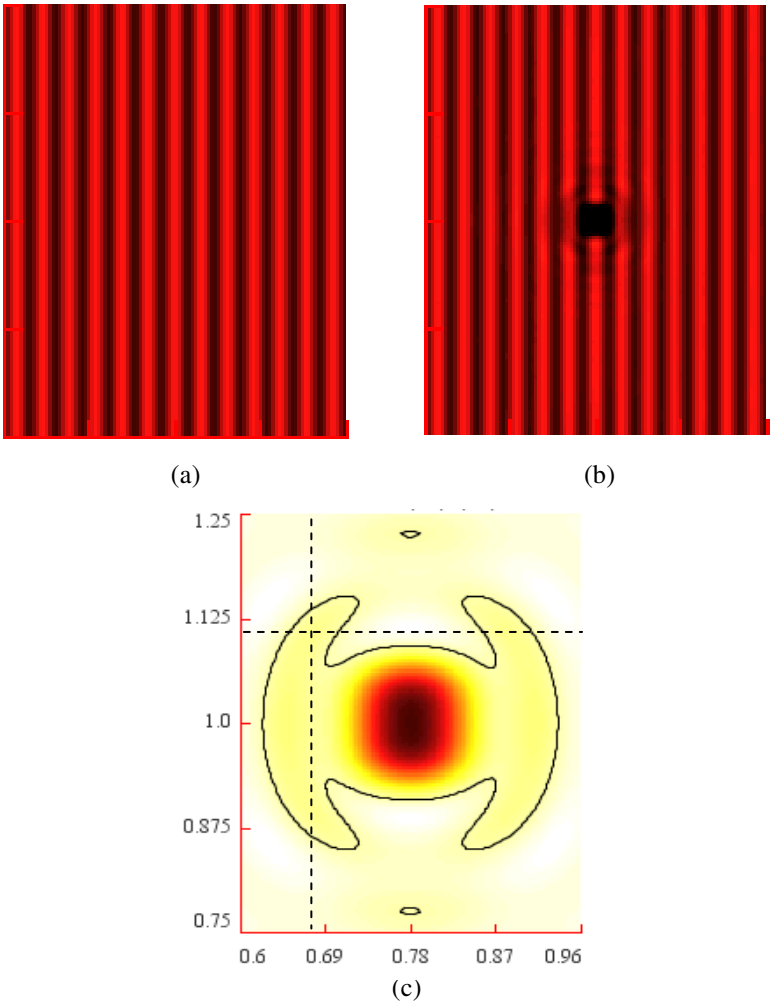


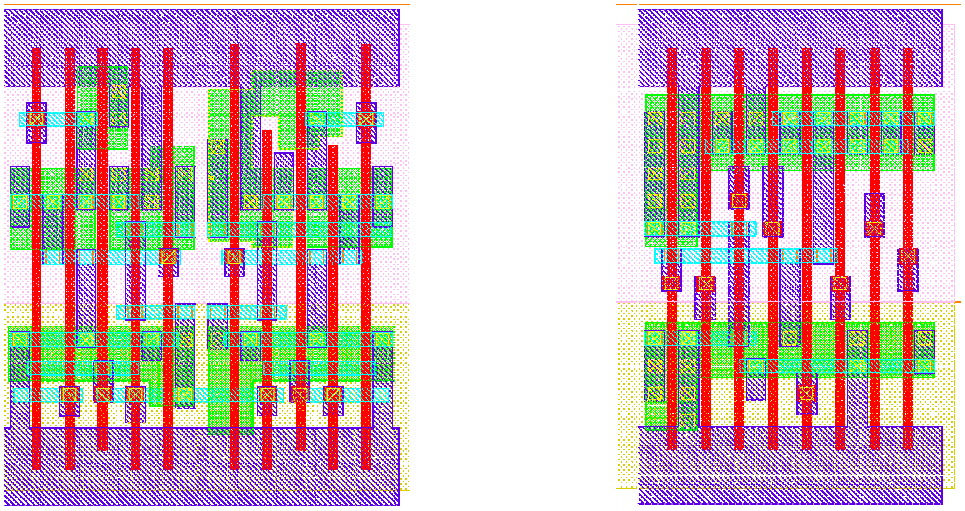
Figure 2: (a) Aerial image of grating (b) Aerial image of line-end in a grating (c) Zoomed in view of perturbation in aerial image caused by introducing a line-end in grating

Using a more realistic optical region of influence to define the patterns found in a regular design fabric leads to a sufficiently manageable number of patterns that can then be used for co–optimization between layout and lithography. The details regarding the raw number and type of patterns observed in regular design fabric is beyond the scope of this paper.

4. CIRCUIT, LAYOUT AND LITHOGRAPHY CO–OPTIMIZATION

In an earlier publication [9], we have already discussed the advantages of regular design fabrics not only for layout and lithography co – optimization but also described the motivation and application of larger functional cells (bricks) in a modified ASIC design flow to enable IC designs that are highly manufacturable without compromising the density or performance of the design. In this work we stated that the layout patterns used to define the regular design fabric must not only be lithography friendly but also circuit friendly. For example, if we can design ICs with only manufacturability friendly patterns such as gratings one could easily enable production k_1 below 0.4. Although a noble goal, it is known to be difficult to design efficient ICs from gratings. Instead we must design with patterns that are "grating–like" but also enable the design of efficient circuits. More importantly, we must also select circuit topologies that are easier to layout using the chosen set of "grating–like" patterns. For example, it is observed that circuits designed using transmission gates based topologies are more difficult to implement using "grating–like" patterns compared to circuits based on AO - based CMOS. Hence the task of enabling next generation lithography processes is one of co-optimization between circuit topologies, layouts patterns and lithography processes. In our proposed methodology we propose to use bricks designed on a regular design fabric to enable process design co – optimization and hence technology scaling.

A major contribution of the work is to determine circuits that can be efficiently mapped to the "grating–like" patterns that lithographers can easily optimize to enable more realistic and pattern specific pushed rules. Fig 3 shows that improvement achieved by co-optimizing the lithography, layout and circuit for a brick compared to co-optimization between layout and lithography only. A 20% transistor count reduction and a 27% area reduction is observed for this brick by circuit, layout and lithography co–optimization.



(a) (b)

Figure 3: (a) Layout of brick implemented using only layout and lithography co – optimization (b) Layout of brick implemented using circuit, layout and lithography co - optimization

We have demonstrated the feasibility of co–optimization between circuit, layout and lithography in commercial 65nm, 45nm and 32nm processes. In [9] we have discussed the validation of pushed rules and also the implementation of 65nm Low Power CMOS ARM926EJ with 20 fixed sized bricks in the same die size and meeting the same performance targets as the reference, while applying extreme regularity enforced by the regular design fabric. This design was tested to be functional at first silicon, significantly cutting the RTL to silicon time and cost. In a second example a 65nm implementation of a PowerPC 405 design was achieved having excellent manufacturability and design advantages [10].

4.1. FEOL Limited Regular Design Fabric

Circuit designers want to find the most efficient way of mapping transistors in a circuit to the transistors in layout. One of the primary necessities is to connect metal 1 polygons to the terminals of the transistor (in active or poly layer) using a contact. As a result, gates (poly over active) in IC layouts most often have a contact between them to access either the source or the drain of the respective transistor. It is imperative that the contacted gate pitch (poly pitch with a contact in between) is the most frequently occurring pitch for the poly layer instead of the minimum poly pitch. In our approach to design circuits with a limited number of grating–like patterns, we have to limit the pitches used for layout design. Since the contacted gate pitch is the most frequently occurring design pitch, we constrain the poly pitch for the FEOL limited regular design fabric to be the contacted gate pitch. Under such a constraint the horizontal scaling of the FEOL limited fabric is limited by the front–end of line rules. Specifically, to achieve higher transistor density we need to solve the integration challenges involved with scaling the contacted gate pitch and do not really care for the printability of the minimum poly pitch. One of the unique pattern restrictions set by this fabric limits the use of horizontally adjacent metal 1 polygons to either connect to an active polygon or to a poly polygon but not both. As a result the FEOL limited fabric requires the staggered metal 1 layout pattern (shown in Figure 4) in order to make the required source, drain and gate connection. Although this staggered metal 1 pattern occurring at half the poly pitch might appears to be a difficult pattern to print, our experience suggests that it is actually a printability friendly and metal line-ends drawn in this configuration can be designed closer to together compared to the pattern where line – ends are abutting each other. Moreover, in the case of the FEOL limited fabric, the metal 1 pitch is the same as the contacted poly pitch. The use of a larger metal pitch shows an improved process window for the metal 1 layer, which is often found to be one of the most challenging layers to print for conventional standard cell layout methodology. In the next section we will discuss the improvement in printability for patterns used in the FEOL limited fabric. It must me noted that the FEOL limited regular design fabric is one of the layout constructs used for industrial designs discussed in the earlier section as it enables efficient layout design of the selected AO – based static CMOS circuit topologies at higher levels of manufacturability.

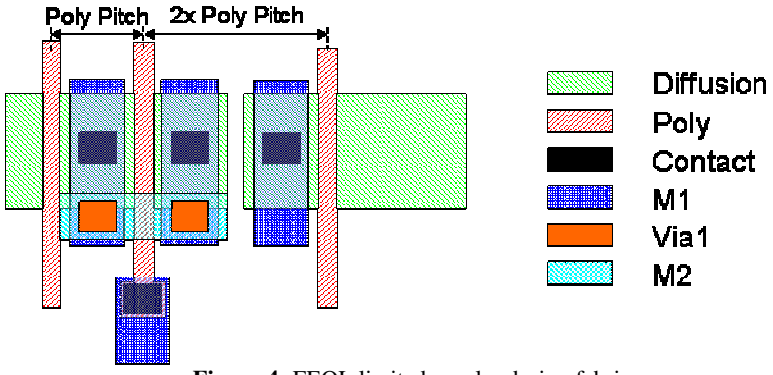


Figure 4: FEOL limited regular design fabric

5. 32nm LITHOGRAPHY FOR REGULAR DESIGN FABRICS

In the previous section we have discussed the pitch relaxation observed for metal 1 patterns in a regular design fabric. In this section we will discuss the printability benefits of using a regular design fabric where the layout patterns are picked to both enable efficient circuit implementation but also lithography optimization.

5.1. k_1 Relaxation for FEOL Limited Design Rule Fabric

Figure 5 shows the k_1 requirements for 32nm metal 1 half-pitch for standard cell layouts using conventional design rules and for a regular design fabric to meet the scaling requirements of 32nm technology node. The data suggests that we would need a metal 1 process that operates at a rather unrealistic k_1 value of 0.33 for layouts created using conventional design rules. More interestingly, with the k_1 relaxation observed for layouts using the FEOL limited regular design fabric we can enable a 1.3NA 32nm metal 1lithography process with a relaxed and realistic production k_1 of 0.4. Additionally a thorough optimization of layout and process can enable 1.2 NA lithography at a more aggressive k_1 of 0.37.

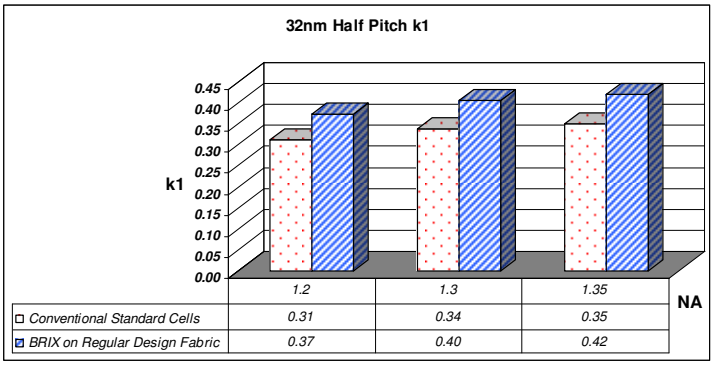


Figure 5: 32nm half – pitch k_1 analysis

5.2. Design Style vs. Process Requirements for Metal 1 Layer

Next we demonstrate the benefits of k_1 relaxation on some realistic 2-dimensional layout patterns. Metal 1 is used to connect the contact terminals between different transistor terminals and via connections to upper level metals. Hence for the metal 1 layer for the design density is dependent on the pitch and spacing between facing line-ends. In our simulation study we focused on the ability to print two metal 1 line-ends closer together. The ability to print two metal 1 line-ends closer together enables the use of two unconnected vias (or contacts) closer together and it turn improved metal 1 density. Fig 5 shows the metal configuration chosen for this experiment. The selection criterion was based on prior experience that suggested such a configuration to have the most line-end pullback from the set of patterns in a regular design fabric.

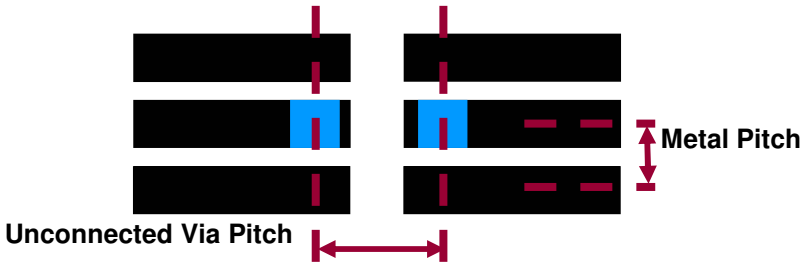


Figure 6: Unconnected via pitch for head-on line-end configuration used for the experiment

Variable	Values
Pitch (nm)	**90,100,110,120,130**
CD (nm)	**40,45,50,55,60,65,70,75,80,85,90**
Drawn distance between line-ends (nm)	**40,50,60,70,80**
Serif (nm)	**0, 10, 20, 30, 40**
NA	**1.2, 1.35**
Illumination type	**Annular, Quasar, cQuad**
Outer Sigma	**0.8**
Inner Sigma	**0.3, 0.4, 0.5, 0.6**
Photomask	**6% attenuated**
Resist Model	**LPM model**

Table 1: Variables explored for process – design co-optimization of metal 1 line-ends

The unconnected via pitch, shown in Figure 6, is the minimum pitch between two vias such that the metal 1 line-ends do not merge as well as provide sufficient coverage of via under a worst case misalignment condition of 12nm. Although

the unconnected via pitch depends on the printability of metal 1, via 1 and metal 2 layers, this analysis only considers the printability of metal 1 layer. Figure 7 illustrates the relationship between metal 1 pitch and unconnected via 1 pitch (purely from metal 1 printability viewpoint) for two different NA tools. In this experiment we have exhaustively explored various OPC strategies and illumination shapes using PROLITH simulator from KLA - TENCOR. Simulations covered a range of process and design variables as shown in Table 1 to determine process and design conditions that provide 200nm DOF, as well as limit the mask error enhancement factor (MEEF) to less than 3.

Results in Fig 7 indicate that a 1.35 NA tool cannot resolve the required conventional design rule minimum metal 1 pitch of 90nm (at a k1 of 0.31) for the line-end pattern under consideration. Technologist have long foregone the hope to have a 90nm metal 1 pitch for the 32nm technology node and are instead targeting a more relaxed 100nm metal 1 pitch. Although a 1.35 NA tool can resolve a 100nm pitch at a k1 of 0.35, it does so at a much more relaxed unconnected via pitch. Hence for the layouts using conventional design rules, which require aggressive scaling of metal 1 pitch and line-ends, a single patterning approach, will not meet the density requirements of the 32nm technology node. The results are consistent with simulations shown in an earlier publication [9] where we demonstrated the challenge with printing the minimum line-end spacing for such a pattern at minimum metal pitch. In the case of the FEOL limited regular design fabric, scaling requirements require the 32nm contacted gate pitch, and hence the FEOL limited fabric metal 1 pitch, to be 120nm. At this metal 1 pitch we only need to optimize the lithography setup to enable aggressive scaling of line-ends so that we can enable an unconnected via 1 pitch of 120nm. It can be observed from Figure 7, that the scaling requirements for metal 1 for regular design fabrics can be achieved with a 1.2 NA system at a k_1 of 0.37. It can be concluded that the smart selection of layout patterns can extend 1.2 NA single patterning optical lithography to a 32nm process.

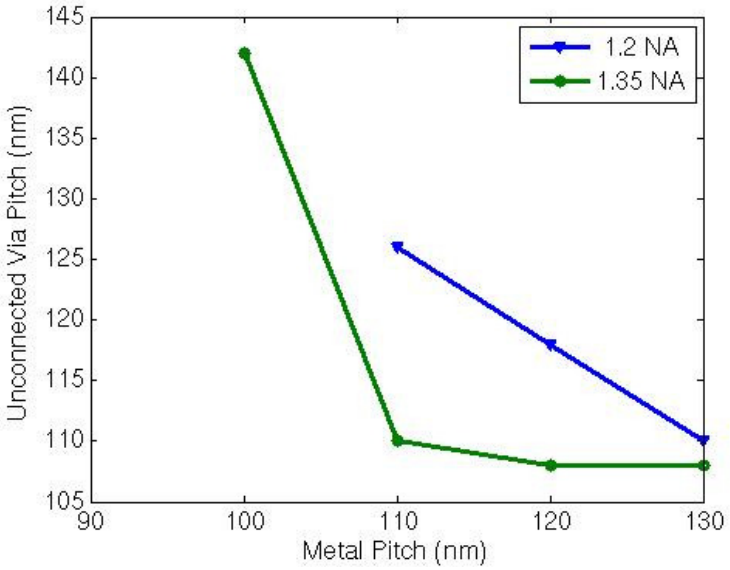


Figure 7: Summary of metal 1 line – end printability for 32nm technology node

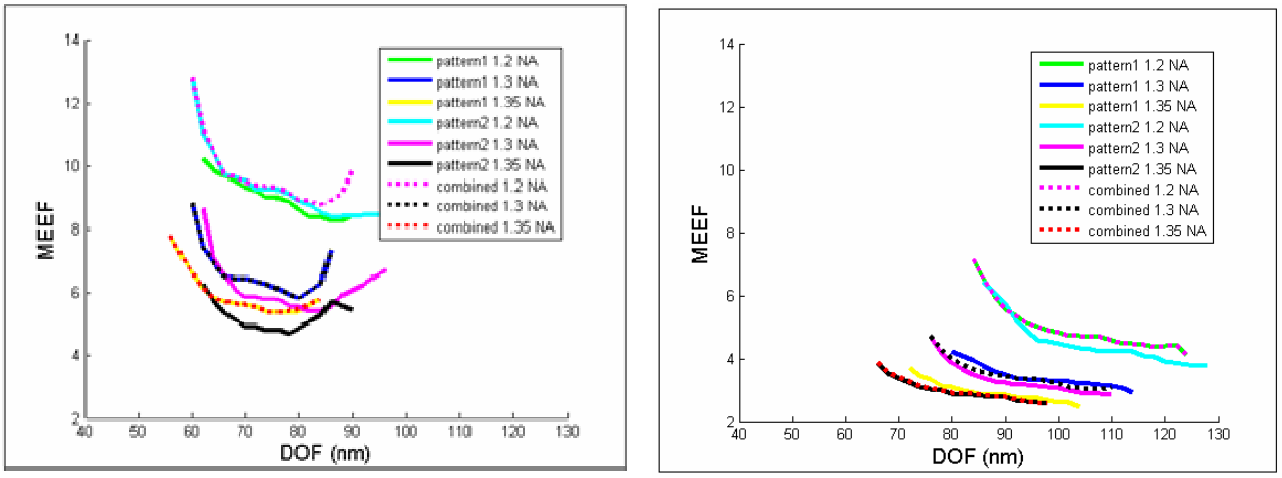
5.3. Design Style vs Process Requirements for Hole Layers

Figure 8: Patterns used for hole simulation

The hole layers (contacts and vias) have been one of the biggest challenges for optical lithography for sub – 100nm technology nodes. It is becoming increasingly difficult to provide 70% linear shrink in pitch for these small holes with sufficient process windows. The use of regular design fabric not only enables a relaxed metal 1 pitch but also a relaxed contact and via pitch. To demonstrate the improvement of k_1 relaxation for holes we performed another set of experiments to exhaustively study the various illumination shapes, photomask types and assist feature strategies in PROLITH. OPC was performed using PROLITH's model based OPC. We studied two of the most frequently occurring and diverse patterns observed in the FEOL limited fabric. The patterns are shown in Fig. 8 whereas the range of process and design variables covered is listed in Table 2.

Variable	Values
Pitch (nm)	**100, 120**
OPC	**PROLITH Model Based with and without assist features**
NA	**1.2, 1.3, 1.35**
Illumination type	**Annular, Quasar, cQuad, Bulls-Eye**
Outer Sigma	**0.6, 0.7, 0.8, 0.9**
Inner Sigma	**0.4, 0.5, 0.6, 0.7**
Polarization	**TE**
Photomask (attenuated Transmission)	**6% , 9%**
Resist Model	**LPM model**

Table 2: Variables explored for process – design co-optimization of hole patterns



(a) (b)

Figure 9: (a) Summary of hole simulations for standard cell (c) Summary of hole simulations for regular design fabrics

Figures 9 (a) and (b) show the summary of the simulations for comparison between lithographic performance for holes in a standard cell design at an x and y pitches of 100nm compared to that in a regular fabric design at an x and y pitches of 120nm. The analysis is performed to calculate the MEEF and DOF for every possible combination of illumination shape, photomask attenuation and assist feature strategy. We then plot the lowest possible MEEF over the range of DOF observed. Hence each point on the graph corresponds to a unique combination of illumination shape, photomask attenuation and assist feature strategy. We plot the lithography behavior of the patterns individually and when considered simultaneously for all the three different NA options. Since both the pattern types occur in circuits implemented using regular design fabrics, it is necessary that we determine process conditions that enable acceptable values of DOF and MEEF for both patterns simultaneously. The trends follow common wisdom and indicate that higher NA tools help reduce the MEEF but degrade DOF. However it is observed that it is not possible to meet the desired MEEF of less than

4 for standard cell designs. On the other hand it is possible to meet the MEEF requirements for regular design fabrics using either a 1.3 or 1.35 NA tool but the lower MEEF is achieved by compromising DOF. For the regular design fabric the optimal trade – off for MEEF vs DOF is achieved by using a 1.3 NA tool, where we can achieve MEEF of 3.5 at a DOF of 110nm. These results indicate the use of regular design fabrics can enable a single exposure lithography solution for holes for 32nm logic applications.

5.4. Summary of the 32nm Technology Node with Regular Design Fabrics

	Conventional Standard Cells	Regular Design Fabric
Poly	1.3-1.35 NA *	1.2-1.3 NA *
Active	1.3-1.35 NA	1.2 NA
Contact	Double Patterning	1.3-1.35 NA +
Metal 1	Double Patterning	1.2-1.3 NA
Via 1	Double Patterning	1.3-1.35 NA
Metal 2	Double Patterning	1.2-1.3 NA

Table 3: Lithography requirements for 32nm technology node

Table 3 shows the lithography requirements for the 32nm technology node for the FEOL limited regular design fabrics and compares it to that of ICs designed using conventional standard cells and design rules. As discussed in the earlier section the application of regular design fabrics can enable use of single exposure lithography for the 32nm technology node for metals and holes, whereas standard cells would not meet the strict 50% area scaling using single exposure lithography. Standard cells would have to move to widespread use of double patterning techniques to meet the requirements of technology scaling. In the case of the poly layer the challenge with printing line–ends for SRAMs would warrant the use of a trim mask. Additionally the need for the minimum poly pitch for standard cells warrants the use of a higher NA tool compared to a lower NA tool for regular design fabrics. The active layer in a regular design fabric has fewer and selective notches and will once again enable lithography with a lower NA tool. Finally, in the case of contact where standard cells would have to use double patterning, it was shown that single exposure lithography for logic designs would suffice for regular design fabrics.

CONLUSIONS

In this paper we have discussed the evolutionary shift of lithography will to a circuit transfer technique. We have demonstrated the use of regular design fabric to enable complete circuit, layout and lithography co – optimization to extend lithography into the future generations. Specifically, we have discussed the strategy of limiting the total number of patterns and creating layout designs that enable both optimization of lithography processes and efficient mapping to circuits. We have discussed the FEOL limited fabric and have shown the lithography benefits observed by k_1 relaxation. Most importantly we have demonstrated the use of single exposure lithography for the 32nm technology node.

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