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Device Array Scribe Characterization Vehicle Test Chip for Ultra Fast Product Wafer Variability Monitoring

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Abstract – Lower supply voltages and aggressive OPC on 65nm and below technologies are causing larger variability of critical device parameters like Vt and Id. With ever increasing clock frequencies, more and more performance related yield loss can be observed even for purely digital circuits. To design more robust circuits it is required to characterize device variability within die, within wafer, wafer to wafer as well as lot to lot. Large samples of device measurements are necessary for accurate variability characterization. A novel Characterization Vehicle (CV) has been developed, which achieves an extremely efficient placement of several hundred devices by arranging them underneath the probing pads. Placed next to product chips, those Scribe CV test chips are providing Vtlin, Idlin, Vtsat, Idsat, Gmlin, and Gmsat for more than 25000 devices per 300 mm wafer requiring less than 20 minutes for testing.

1 Introduction

For 65nm technologies and below, it is required to characterize much larger device sample sizes. There is a stronger impact of layout pattern on device performance due to strong OPC and focus and exposure variability. 300mm wafers show more significant spatial trends than in previously technology nodes. It is simply impossible to characterize all those effects by just looking at a few devices on 5, 9 or 15 dies per wafer.

Device arrays have been introduced to improve area usage and allow larger design of experiments (DOE). [LeJa03], [ScLT00], [SMCS04], [ScEi05] describe just a few of those. However, even if the number of devices per die can be increased, test time is the ultimate bottleneck in collecting the required data from much larger sample sizes. Lately, analog measurement systems are being introduced that provide significantly higher number of parallel measurement channels. However, none of the existing device array architectures truly support massive parallel testing.

Thus, we are introducing a comprehensive wafer level variability monitoring system, which will enable high volume sampling within given area and test time budget.

2 Test Chip Design

A novel transistor array architecture is introduced to achieve maximum area efficiency and simplicity in addressing a device under test as well as supporting parallel testing.

2.1 Maximizing Area Efficiency

The proposed device array will pack 32 devices within an array, where all routing just requires two metal layers. Thus, the array can be placed underneath the pads, which are implemented in Metal 3 and above. The left side of Figure 1 illustrated this approach.

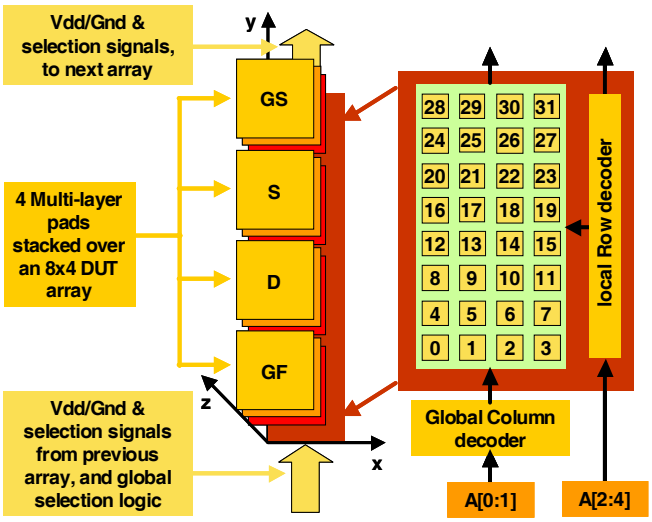

Figure 1: Concept of arranging 32 devices (right) under probe pads (left).

2.2 Simplicity in Addressing a Device Under Test

The proposed array has 32 devices under test (DUT), which share the source and drain pins. There are no selection devices in the source and drain path, which is important to gain accurate measurements. Furthermore, it eliminates the risk of back-biasing wells, which can easily happen, if a selection device is implemented along the pad to source path. Smart and balanced routing limits the

resistance between each pad and the source or drain pins of each DUT to 5 ohms. In the device array presented here, the only selection device is being used in the pad to gate path to turn on a specific DUT. For the gate pin, a force and sense path is being used to monitor and adjust the gate voltage if required. The selection logic is purely combinatorial as indicated at Figure 2 and it is being shared among several arrays. The absence of timing critical circuitry reduces design time, simplifies testing and ensures a very robust design among a variety of technologies.

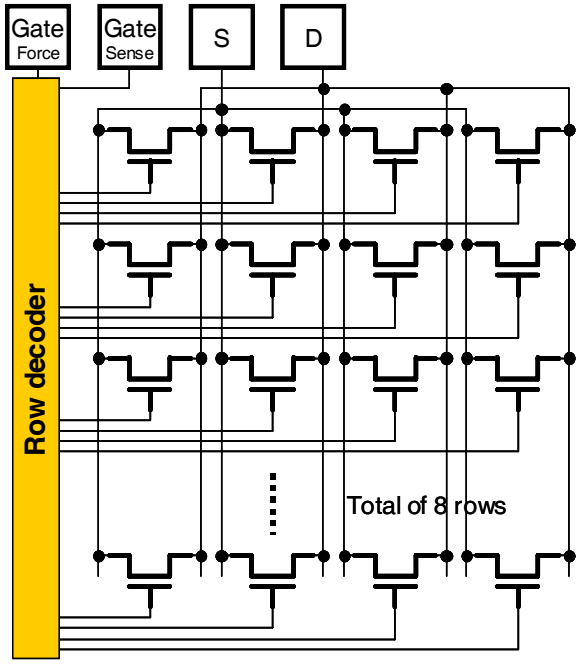

Figure 2: Schematic of one array the Device Scribe CV test chip.

2.3 Support of Parallel Testing

As shown in Figure 3 on the right, 10 such arrays are implemented in one pad group to be tested in parallel. The Device Scribe CV® Test Chip or simply dScribe CV can then be placed in one or more locations on a reticle next to product chips as shown on the left side of Figure 3.

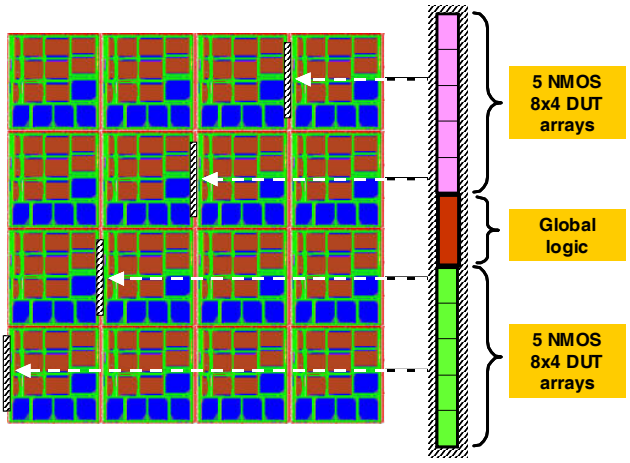

Figure 3: Packing of arrays into one Scribe CV Test Chip (right) and potential placement on a multi product reticle (left).

3 Experimental Results

dScribe CV Test chips are being implemented within the scribe line of product wafers. A layout example can be seen in Figure 4. The center section is shown on the left. The center 8 pads are used for power supply and address bits driving the common logic for 10 arrays each holding 32 devices. Each array is placed under 4 pads as can be seen in the center of Figure 4. The right side shows the placement of 8 devices under one single pad.

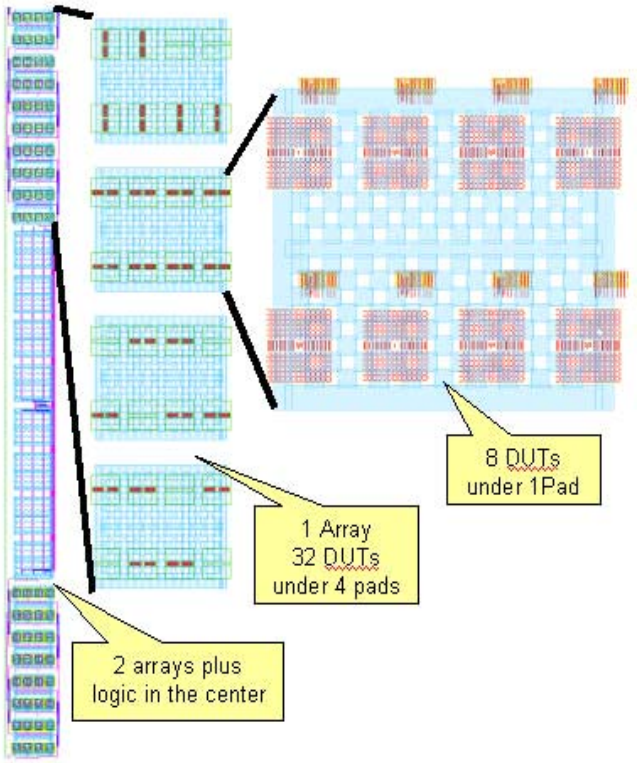

Figure 4: Zoom in from left to right within a layout example of a Device Scribe CV Test Chip.

3.1 High Speed Testing using pdFasTest II

In general, testing can be executed as early as the first metal layer with pads has been manufactured. Dependent on the ILD thickness and softness it is recommended to start testing one or two metal layers higher to ensure robust test results if probing related stress shows an impact.

The pdFasTestII® test system is being used to test the dScribe CV Test chip. It provides up to 72 parallel analog testing channels. The 10 arrays of the dScribe CV are being tested in parallel. Within each array, the 32 devices are tested in sequence. pdFasTestII just needs 11 seconds to obtain two I/V curves for each of the 320 devices, one for linear region and one for saturation region. From those curves, the tester derives key device parameters like Vtlin, Idlin, Vtsat, Idsat, Gmlin, and Gmsat. A regular parametric tester needs for the same task 11 minutes, which translates into a test speed gain of 60. Despite the large speed advantage, correlation of test results is excellent as can be seen in Figure 5 and Figure 6.

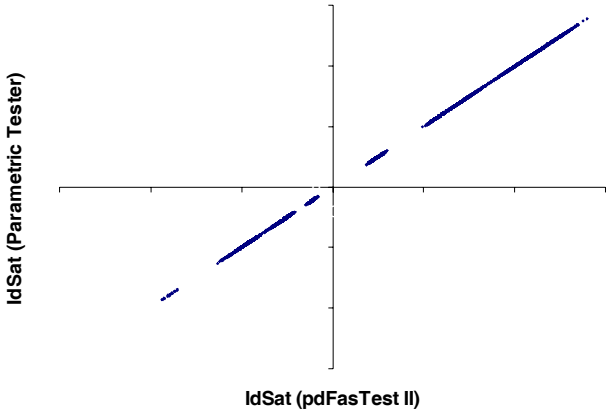

Figure 5: Comparison of Id measurements taken with pdFasTest II and a standard parametric test system.

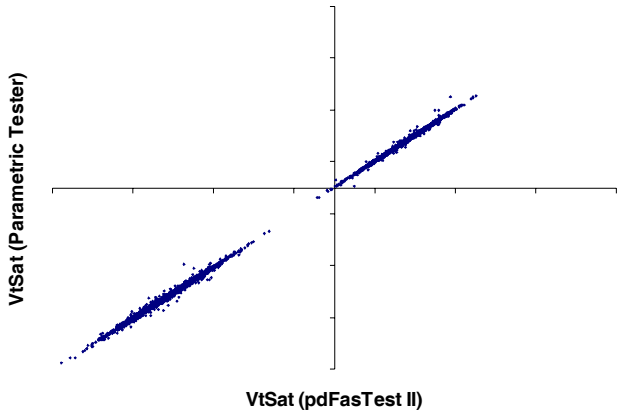

Figure 6: Comparison of Vt measurements taken with pdFasTest II and a standard parametric test system.

3.2 Data Accuracy

To evaluate the accuracy of data taken from a device array as suggested in this paper, we have implemented identical transistor layouts on a FEOL CV twice, once connected within the device array and once connected straight to individual pads. Direct comparison between the individually padded transistors and the arrays is difficult, because they are on different locations of the wafer and across chip variation between the two locations creates a difference between the two sites. The correlation between the arrays and individually padded devices is evaluated by comparing the distributions of the two sets of measurements by means of a probability-probability (P-P) plot. Figure 7 is an example P-P plot for Idsat, showing good agreement of the device array and individually padded transistor distribution. Thus, using pdFasTest II to measure the proposed device array is a very powerful solution to increase sample size by simultaneously decreasing test time.

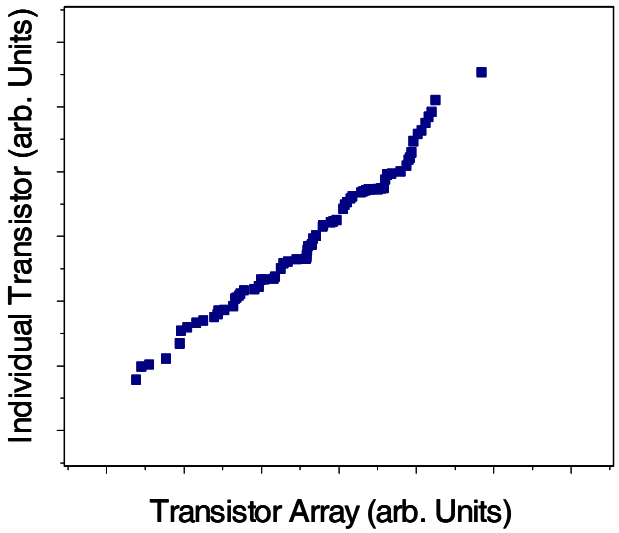

Figure 7: Comparison of Id data from identical transistor layouts taken either from a device array or devices connected straight to the pads.

3.3 Applications

The dScribe CV Test chip in conjunction with the pdFasTestII fast parallel testing provides a very large sample of transistor measurements with minimal test time. It enables the testing of more than 300 transistors on all wafers and all die on a 300 mm wafer. This volume of data enables many applications that are not feasible with limited parametric data available from standard process control monitor (PCM) testing, typically 9-15 die on a wafer.

The effectiveness of combination of transistor arrays and pdFasTestII® testing was evaluated by comparing the transistor measurements obtained from a dScribe CV with conventional individually padded process-control monitor (PCM) structures. Figure 8 shows a typical Vth-Idrive comparison. The dScribe CV measurements are in good agreement with the PCM measurements from a typical parametric tester. In addition, the much larger sample of data available from dScribe CV, provides a better estimate of transistor performance variability than available from PCM measurements typically taken on the same wafers.

The much larger measurement sample size available from dScribe CV also allows a better decomposition of the transistor performance variation into within wafer spatial components and other sources of variation like wafer-to-wafer and lot-to-lot variation. For example, Figure 9 shows examples of spatial patterns we have observed in dScribe CV measurements from production wafers that contribute to across-wafer non-uniformity. Such detailed characterization of across-wafer non-uniformity is not possible with typical PCM sampling plans.

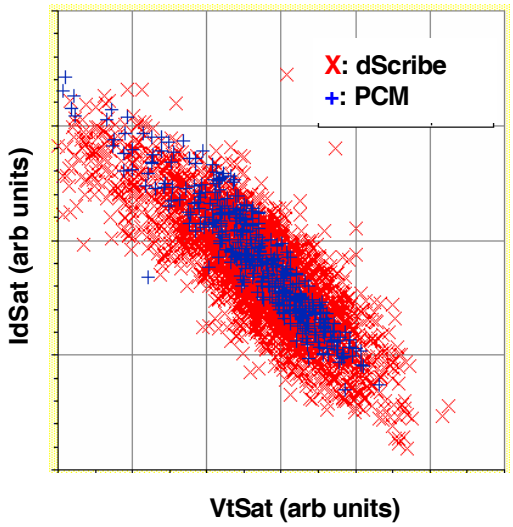

Figure 8: Comparison of dScribe CV measurements with standard PCM measurements from a parametric tester.

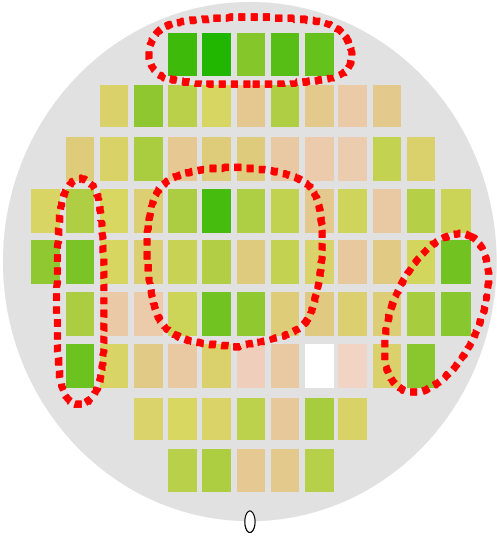

Figure 9: Spatial patterns of device performance revealed by full wafer sampling.

Further applications of the dScribe CV include: detailed spatial analysis of across wafer non-uniformity of transistor performance, correlation of transistor performance to product yield to quantify and understand transistor related yield loss, excursion monitoring, automated signature analysis of spatial patterns. Moreover, in conjunction with additional inline data and equipment logs this data can be used to find equipment level root causes for excursions.

For example, Figure 10 shows the spatial pattern observed on a set of excursion wafers with a large number of non-functioning devices. Examination of the spatial pattern of the failing devices helps identify root causes of such excursions. Figure 11 shows the distribution circuit delay figure of merit (FoM) obtained from a large sample of dScribe CV based measurements. The large population provides a more accurate estimate of the delay distribution than would be possible with typical PCM measurements. For example, the slow tail, which would result in slow parts, can be seen in the dScribe CV measurements and is not apparent with a much reduced sampling.

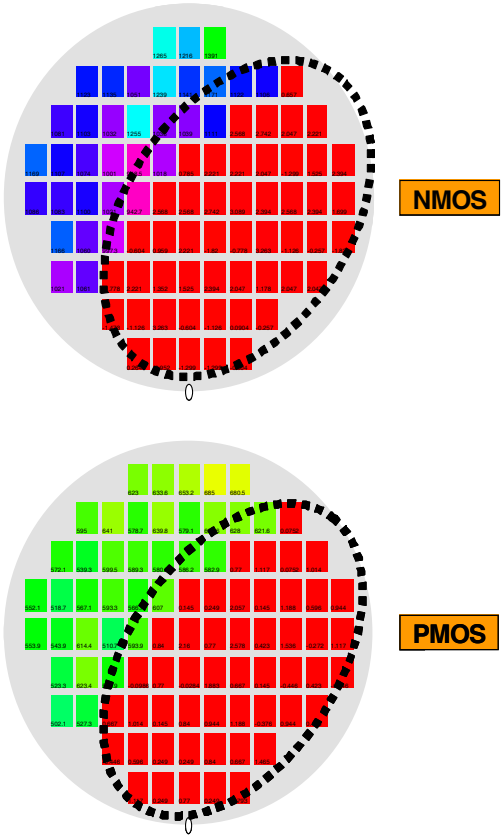

Figure 10: Spatial pattern observed on a set of excursion wafers with a large number of non-functioning devices (NMOS left; PMOS right).

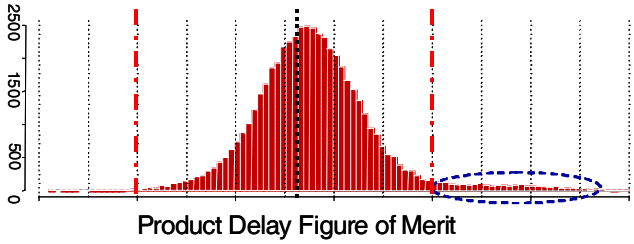

Figure 11: Large sample size of device measurements allows estimation of tails in the performance distribution.

4 Conclusion

Compared to conventional single padded devices placed in a scribe line, the Device Scribe Characterization Vehicle Test Chip based monitoring system provides more than 1000 times more data by maintaining the same area (32x gain) and test time (60x gain) budget. It is a very fast, robust and comprehensive system to characterize device variability. The dScribe CV is placed next to product chips. Parallel testing using pdFasTest II provides Vtlin, Idlin, Vtsat, Idsat, Gmlin, and Gmsat for more than 25000 devices per 300 mm wafer in less than 20 minutes without compromising data accuracy. The dramatically increased sample size enables detailed correlation of transistor performance to product yield data to better understand transistor related yield loss including excursion monitoring and automated signature analysis of spatial patterns.

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