# ANALYSIS OF THE IMPACT OF PROCESS VARIATIONS ON CLOCK SKEW

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*Abstract*— **In this work we analyze the impact of process variations on the clock skew of VLSI circuits designed in deep sub-micron technologies. With smaller feature size, the utilization of dense buffering scheme, has been proposed in order to realize efficient and noise-immune clock distribution networks. However local variance of electrical MOSFET's parameters, such as $V_T$ and $I_{DSS}$, increases with scaling of device dimensions, thus causing large intra-die variability of the timing properties of clock buffers. As a consequence we expect process variations to be a significant source of clock skew in deep sub-micron technologies. In order to accurately verify this hypothesis we applied advanced statistical simulation techniques and accurate mismatch measurement data in order to thoroughly characterize the impact of intra-die variations on industrial clock distribution networks. The comparison with Monte Carlo simulations performed neglecting the effect of mismatch confirmed that local device variations play a crucial role in the design and sizing of the clock distribution network.**

*Keywords*— ************* INSERT KEYWORDS *************

## I. Introduction

The design of the clock distribution network is a critical task because the performance and functionality of synchronous systems directly depend upon the clock signal characteristics. At the same time the logical and physical design of reliable synchronization circuitry involves the combined optimization of multiple conflicting objectives such as bounded skew, noise immunity, low power consumption, area etc. Because of this, the automatic synthesis of the clock tree network has gained a considerable attention in the design community; a comprehensive overview can be found in [1]. The problem of generating a zero-skew or a bounded skew routing tree is of primary importance for high speed logic design. Existing clock tree routing techniques [2-7] are based on linear or Elmore delay [2] metrics to approximate the signal delay in every tree branch. This approximation is provably a worst-case delay estimation for RC trees [3]. Unfortunately this upper bound is often considerably loose [2], especially for long interconnect wires routed in Deep Sub Micron (DSM) multiple metal layers technologies. Thus, in order to maintain a reasonable level of accuracy it is thus necessary to make extensive use of buffers throughout the clock tree.

On the other hand it is possible to expect that the introduction of a large number of buffers will make the tree more sensitive to intra-die process variations, particularly if the effect of buffer delay mismatch is not taken into account by the clock tree synthesis algorithm. One of the earliest attempt of accounting for the effect of process variations on the skew has been proposed in [4]; however only global process corner variations have been considered in this work. In [5] the effects of both interconnect and buffer intra-die variations have been incorporated in an algorithm for reliable clock tree routing; however the authors in [5] used a simplified buffer delay model (k-factors) and the effect of local variations was taken into account only by empirically varying the k-factors of $\pm 10\%$. Xi and Dai[6] considered only global process variations (fast and slow corner combinations for PMOS and NMOS devices) and used global derating factors, thus ignoring the effect of local variations. Finally, authors in [7] have included the effect of intra-chip, long range gradient variations in an analytical model of the skew of a pipelined H-tree. As the information regarding the individual position and orientation of a chip on the wafer is lost after wafer dicing, the model derived in [7] may be difficult to apply in practice. Moreover, it is shown in the present work that the usually neglected component of mismatch that is proportional to the inverse of the channel area tends to dominate in DSM technologies.

To our knowledge this is the first work in which a thorough experimental characterization of statistical variability is applied to the accurate analysis of the effect of device mismatch on the clock skew of VLSI IC's. In fact, as far as we know, no systematic characterization of the mismatch has ever been run. We will compare the results of accurate statistical simulation including respectively the effect of global variations, area dependent mismatch and area and distance dependent mismatch on the clock skew for two industrial strength circuits:

- a Graphic Processor Unit (GPU) for consumer applications
- a DSP core (Viterbi decoder)

all designed by using a standard design flow in 0.25 $\mu$m CMOS technology.

By using these significant examples, we will show that both global and local, area-dependent process variations may have a considerable impact on the performances clock skew, and that they have to be properly modeled and taken into account for reliable, high-speed clock tree synthesis.

## II. MISMATCH MODELING AND SIMULATION TECHIQUE

Significant efforts has been spent in the past in the modeling and characterization of mismatch effects [8][9][10][11][12][13][14], but the lack of an effective statistical simulation methodology, incorporating mismatch effects [15], has prevented a widespread application of mismatch analysis to large circuits. In fact, a straightforward application of any device mismatch model in Monte-Carlo analyses, usually leads to an unrealistic amount of circuit simulations.

In this section we first introduce the mismatch model used throughout this paper, then we present the adopted simulation technique.

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### A. Mismatch Modeling

From now on we will address to the mismatch between two or more devices as the difference among their (ideally identical) electrical parameter values. Such a simple definition does not provide the engineer with a deep understanding of the real sources of the aforementioned variability, however, in order to serve our purposes it is sufficient to recall that the causes of device mismatches, which are pseudo-random in nature, can be divided into two main categories: systematic and random. Obviously, the choice of the mismatch model is constrained to those which include both of these components.

Although several corrections and extensions to the DSM region, such as those presented in [9], [12] and more recently in [16] and [13], have been proposed, the model proposed by Pelgrom et. al. [8] is still the most widely used in the current practice.

********** FIGURE 1 ***************

Fig. 1. Definition of geometrical terms used in the Pelgrom model.

Pelgrom's model describes the variance of the difference of the value of a generic parameter $p$ in two identically drawn, rectangular devices, T1 and T2 ($\Delta p = \rho_{T_1} - \rho_{T_2}$), with length L and width W whose distance between their centers is $d$ (Fig. 1)************** as:

$$\sigma^2_{\Delta p} = \frac{A_p^2}{WL} + S_p^2 d^2, \tag{1}$$

where $A_p^2$ and $S_p^2$ are the fitting parameters for the area and the distance dependent terms, respectively. They are extracted directly from process characterization data.

In general, in order to account for process variability, it is possible to describe the *i-th* electrical parameter (e.g. $V_T$, $\beta$, $\mu_0$, etc.) of the *j-th* MOS device ($P_j^i$) as the sum of three different components:

$$P_j^i = \mu_{P^i} + g_i + m_j^i, \tag{2}$$

where $\mu_{P^i}$ is the mean of $P^i$, $g_i$ and $m_j^i$ are random variables with zero mean and variance $\sigma_{g_i}$ and $\sigma_{m_j^i}$ respectively.

In (2) $g_i$ accounts for the global variability (in other words that relative to wafer and lot level variance), while $m_j^i$ accounts for local (intra-die) process variability (mismatch). Without losing generality, it is possible to assume that the parameters $P_j^i$, $\forall i, j$ are mutually independent, so that the only non-null correlation terms are those between the same parameter of different matched devices. In fact, as shown in [17], it is always possible to transform the initial parameters set into a corresponding set of independent random variables by using proper statistical techniques (Principal Component Analysis[18]). The non-null correlation terms are not directly available from the process characterization data, as usually the variance of the difference is characterized. However, by using the model proposed in [8]:

$$\sigma^2(P_k^i - P_j^i) = \frac{A_{P^i}^2}{WL} + S_{P^i}^2 d_{k,j}^2. \tag{3}$$

It is possible to demonstrate[19] that the covariance between the same parameter of a pair of identical devices satisfies:

$$k_{P_k^i, P_j^i} = \sigma^2_{P^i} - \frac{1}{2}\left(\frac{A_{P^i}^2}{WL} + S_{P^i}^2 d_{k,j}^2\right), \tag{4}$$

where $A_{P^i}^2$ is the coefficient of the area-dependent mismatch component for parameter $P^i$, $S_{P^i}^2$ is that of the spacing-dependent component and $d_{k,j}^2$ represents the layout distance between *k-th* and *j-th* devices.

The covariance terms in (4) are then stamped in the covariance matrix $\Sigma_{P^i}$ which will be finally used to generate a set of properly correlated samples for the Monte-Carlo simulation as described in the next section.

### B. Correlated sampling

In order to investigate the effect of process variations on clock skew, a set of Monte-Carlo SPICE simulations of the clock network is performed. It is therefore necessary to generate a large number of correlated samples for the relevant SPICE parameters of all the buffers in the tree, where the correlation stems from the intra-die variability. The Cholesky decomposition is been used as in [17] to generate a set of correlated random samples for the Monte-Carlo analysis with the desired covariance matrix. In vector notation equation (2) can be written as:

$$\boldsymbol{P} = \mu_{\boldsymbol{P}} + \boldsymbol{L}_b \boldsymbol{u} + \boldsymbol{L}_m \boldsymbol{v}, \tag{5}$$

where $\boldsymbol{P}$ is a random vector of n correlated variables with mean $\mu_{\boldsymbol{P}}$ and covariance matrix $\Sigma$, $\boldsymbol{u}$ and $\boldsymbol{v}$ are independent random vectors with zero mean and unit variance, and $L_{\boldsymbol{g}}$, $L_{\boldsymbol{m}}$ are lower triangular matrices obtained from the Cholesky decomposition of two block-diagonal covariance matrices ($\Sigma_{\boldsymbol{g}}, \Sigma_{\boldsymbol{m}}$) associated with global and local variations respectively. From the independence of $\boldsymbol{u}$ and $\boldsymbol{v}$ the following relation between $\Sigma$, $\Sigma_{\boldsymbol{g}}$ and $\Sigma_{\boldsymbol{m}}$ holds:

$$\Sigma = \Sigma_{\boldsymbol{m}} + \Sigma_{\boldsymbol{g}} \tag{6}$$

which expresses the intuitive fact that the total variance of each parameter is originated by the superposition of independent global and local physical effects.

In practice, rather than using (5) it is more efficient to directly extract one single random vector with covariance matrix $\Sigma$. Because of the finite population size, the sample mean may not actually be 0. In this case it is possible to subtract the sample average from all the generated vectors in order to obtain unbiased estimations.

### C. Unified Compact Representation of Inter-die and Intra-die Variability

The mismatch simulation methodology described in Section II.B becomes rapidly impractical when the product of the number of matched transistors by the number of independent process factors exceeds few hundreds. In fact, the number of Monte-Carlo runs that would be required in order to obtain a sample with sufficient statistical significance is certainly very large (conceivably more than a few thousands simulations), while at the same time an approach based on RSM performance macromodeling, such as those presented in [15-17], cannot be applied because of the exponential complexity of the Design Of Experiments (DOE) step. As the clock network circuitry may easily contain several hundreds of buffers, an alternative approach is required to study the effect of intra-die variations on the clock network. In our study we decide to use the methodology described in [20] and implemented in Circuit Surfer [15]. This technique exploits the correlation between different device parameters within a given component type (e.g. NFET, PFET, etc.), and that between similar parameters in different matched

devices, in order to decompose the total (inter-die and intra-die) variability into a few independent, dominant sources of variance. This is achieved by an iterative application of Principal Component Analysis (PCA) [18] to a suitably reordered representation of the system correlation matrix:

(7) ********************* MATRIX HERE ****************************

******* REWRITE where the rows and columns () correspond to the parameter of transistor, and thus the element represents the correlation between and and . The correlation coefficients are directly obtained from process characterization data.************* In this way it is possible to obtain a structured, unified representation of both interdie and intra-die variability. This unified model can be simulated with a number of independent variables that, in the worst-case, is linear with the number of matched transistor (but with a much smaller constant than other existing approaches), and that in most practical cases [1] only requires a small constant number of additional independent variables. The number of independent variables is function of the maximum error the user is willing to tolerate. In [20] it is shown that by setting the screening (minimum precision) even to a very high value requires a small number of simulations. It must also be noted that the higher the correlation between the variables, the lesser the number of independent factors necessary to achieve a certain screening value.

## III. MISMATCH SIMULATION OF INDUSTRIAL CLOCK TREES

### *A. Clock skew and related timing measurements definition*

The intra-die variability analysis methodologies described in the previous sections have been used to analyze the impact of buffer mismatch on two different industrial clock tree networks test cases. The relevant timing measurements that have been measured in this work are:

- Data-path delay ($t_d$);
- Slack between data and clock arrival time ($t_{slack}$);
- Clock skew ($t_{skew}$)

In order to guarantee the correct functionality of a synchronous logic circuit, a well defined set of timing con- straints have to be satisfied, as described by the following set of inequalities:

$$T_c - (t_s + t_{skew}) \geq t_d \tag{7}$$

$$t_d \geq t_h + t_{skew} \tag{8}$$

where $T_c$ is the clock period and $t_s(t_h)$ the setup(hold) time of the sequential cells (FF/latches) used to sincronize the data. Note that both $t_{skew}$ and $t_s(t_h)$ can assume either positive, zero or negative values, which implies that the worst-case value is tacitly assumed in (7) and (8). The relations between te different timing measurements used in our examples are illustrated in ******fig. 2********

Fig. 2. Illustration of timing measurements

### *B. Monte Carlo simulation of the Viterbi decoder*

The statistical simulation methodology described in Section II.B has been implemented by using SIMPILOT [21] and C++ language code and applied to study the skew of three different clock-tree networks (clock_bmu, clock_bmu_n and clock_sys) of a Viterbi Decoder designed in a 0.25 $\mu$m CMOS technology. Even though these networks are relatively small, they are representative of a reasonable block size for which it is possible to avoid local re-synchronization of the clock signal. Moreover it was necessary to identify a set of realistic clock networks that could be managed by the statistical simulator in an acceptable time. The net clock_bmu is composed by a single level of 16 buffers driving a total of 910 flip-flops. The net clock_bmu_n is composed by one inverter followed by one buffer driving 4 identical branches, each composed by an inverter-buffer couple. This net drives 40 flip-flops. Finally the clock_sys net is split in 2 branches. The first is made by an inverter-buffer couple driving 4 buffers, and the second by a couple of buffers with a fan-out of 16. This net drives 640 flip-flops. In every buffer, all the devices have the same size and, ideally, they are all perfectly matched. The Viterbi decoder has been synthesized from an RT description on a 0.25 $\mu$m CMOS standard cell library by using Design Compiler [22]; the physical layout has been obtained by using Silicon Ensemble [23] and the clock tree routing has been automatically synthesized by using CT Gen[24]. In order to reduce the size of the problem we decided to model the process variability by using VTN and VTP variations only, based on a buffer delay sensitivity analysis. In order to separate the effects of global variations, area dependent mismatch and layout distance dependent mismatch, the following set of statistical simulation has been performed:

- Nominal;
- Monte Carlo analysis with global variations only;
- Monte Carlo analysis with global variations and area-dependent mismatch ($A_p^2/WL$);
- Monte Carlo analysis with global variations, area-and distance-dependent mismatch ($A_p^2/WL + S_p^2 d_{k,j}^2$).

The fitting coefficients were directly available from the process characterization data. Given the extremely low value of the inter-die mismatch coefficient, we decided to use an higher value for that. The reason for this, is the assumption that the inter-die mismatch plays an negligible role in this clock network. Thus, if for a large a negligible effect is observed, the actual effect will be negligible as well.

The Monte Carlo analyses have been performed by using 1,000 random samples and extracting the clock skew value from transient SPICE-level simulations of the clock network.

### *C. Monte Carlo Simulation of the Graphic Processor Unit*

The second test circuit analyzed in this work is a Graphical Processor Unit (GPU), also fabricated in a 0.25 $\mu$m CMOS technology and designed by using a traditional ASIC design flow. This is a very large circuit (few million gates, more than 2cm die size), for which the application of standard mismatch simulation methodology such as that applied in the Viterbi test case, resulted unfeasible, even when considering only a small partition of the entire clock network. Therefore we decided to apply the more advanced mismatch analysis technique described in Section II.C in this case. The process data indicated that mismatch of was the major source of intra-die variability for this kind of process. The timing properties of the clock network relative to the GPU interface unit, as described in Section III.A have been measured. Four different experiments were performed:

- Global variations only (16 simulations);
- Global variations and local variations (correlation 0.995, screening 99.5
- Global variations and local variations (correlation 0.985, screening 98.5

[1] The worst-case corresponds to a process where all the fabricated devices behave as if they were completely independent (very poor matching), which is, of course, extremely unrealistic. The best-case corresponds to perfect matching (no additional variables required). The most common case is that of slightly imperfect matching (the values in the correlation matrix are all close to 1), corresponding to a small number of additional independent variables.

The high correlation coefficients that have been used in this example, are typical of a process with very good (Analog-like) device matching properties. Therefore any impact of intra-die variability that will be observed is significant, as in general we would expect standard CMOS digital processes to have worst device matching performance.

## IV. Experimental Results

### A. Viterbi Decoder

The results of the set of statistical simulations performed on the clock networks described in Section III.B are summarized in Table I. It is possible to observe that the effect of area-dependent mismatch on the skew is about one order of magnitude larger that associated with global variations only. It is also interesting to note that the introduction of the component of local variance proportional to the layout distance between buffers does not seem to have a sensible effect on the total skew variance. In fact, as reported in Table I, the difference between the simulations performed with and without its contribution can be considered negligible. It is important to note that:

- Since the characterized values of the coefficients were basically negligible for the technology considered in this paper, we decided to use a larger value obtained from the characterization of a previous 0.5 $\mu m$ CMOS technology. The results reported in this work about the effect of distance-dependent mismatch are thus pessimistic and have to be considered as worst case results.
- The actual block size (less than 2mm), obviously, is such that mutual buffer distance is always relatively small in our examples. This has to be considered when analyzing the conclusions about layout distance-dependent mismatch effect.

TABLE I
Range of variations ($\pm 4\sigma$) of clock skew for the clock networks analyses in this work. Values are expressed as percentage variation with respect to the mean.

| Clock Network | Global Variations | Global and Area Mismatch | Global, Area and Distance Mismatch |
|---|---|---|---|
| bmu | 0.96 | 22.24 | 22.24 |
| bmu_n | 2.16 | 19.44 | 18.32 |
| sys_B | 0.80 | 26.24 | 25.84 |
| sys_C | 2.40 | 30.16 | 31.52 |

The results presented in this paper are further confirmed by the histograms shown in Fig. 3 where the effect of global variations (i.e. by setting $v = 0$ in (5)), area-dependent (i.e. by setting i$S_p^2 = 0$ in (3)), and by using the full model of variance described in (5), on the skew of the largest clock tree network (*clock_bmu*) are reported. Finally it is important to note that, even though for practical reasons the contribution of other process variables (e.g. $\beta$, $\mu_0$ etc.) has been ignored, the results about the large impact of mismatch on clock reliability still hold. In fact, the introduction of extra sources of variance may only magnify the spread of the skew. This is additionally substantiated by the fact that the parameters used in this work are those that have the largest impact on the buffer delay, as confirmed by a sensitivity analysis.

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Fig. 3. Histograms of the skew resulting from statistical simulations of clock_bmu including: global variations (a), global and area mismatch (b), global, area and distance mismatch (c)

### B. Graphic Processor Unit

The results of the simulations performed are reported in Table II. It is possible to observe that the effect of the global variations are one order of magnitude greater than the effects of intra-die variations. This is not actually unexpected, because the loads in the clock network are not well balanced. This leads to an increased effect of the global variability that would not be normally observed. It is important to note that:

- The uncertainty on the slack is much greater than the other two cases. In fact, the slack is influenced by both the clock skew and data timing uncertainty. Its value, anyhow, it is possibly due to the fact that the process is not yet stable.
- The uncertainty on the clock skew is smaller than the one found before. This is possibly due to the fact that the correlation coefficient used are maybe too high. for a digital design case. A smaller coefficient should be used to make the simulation more realistic. In this case, the result shouldn Rt be very different from the one found in the previous section.

TABLE II
Variance of the experiments with respect to the nominal case.

| | Exp.a | Exp.b | Exp.c | Exp.d |
|---|---|---|---|---|
| Clock Skew | 26.2 | 26.2 | 26.7 | 26.7 |
| Path Delay | 13.6 | 13.7 | 13.9 | 13.9 |
| Path slack | 51.4 | 52.1 | 52.6 | 52.6 |

## V. Conclusions

In this paper we have analyzed the impact of intra-die process variability on the clock skew of VLSI blocks designed in DSM technologies. In order to incorporate the measured matching data into accurate Monte-Carlo statistical simulations of the clock network, advanced techniques have been applied.

A set of correlated random samples have been generated by using the Cholesky decomposition of the covariance matrices relative to inter- and intra-die variations. This methodology has been applied to study the effect of process variations on the skew of three different clock trees of a VLSI macro-cell (Viterbi Decoder) implemented by using a standard commercial design flow and an industrial DSM standard cell library. The experimental results have shown that for the Viterbi decoder:

1. Global process variations have a negligible effect on the clock skew. This is possibly a consequence of the fact that the wire widths and the buffer loading have been properly sized and balanced.
2. Skew variance due to the local (intra-die) mismatch effect is about one order of magnitude larger than that due to global variations
3. The effect on the skew variance of the component of local variability due to layout distance $S_p^2 d^2$ is negligible compared to that of the area dependent component $\frac{A_p^2}{WL}$.

Therefore it seems to be necessary to model and take into account the area-dependent device mismatch for reliable, bounded skew clock tree synthesis of circuits designed in DSM technologies.

The technique outlined in Section II.C has been applied to the clock tree GPU. In fact, the size of the circuit and the number of transistors to be matched make impossible to apply any direct MC method. The experiments have shown that the effect of inter-die variations are of an order of magnitude greater than the intra-die variations.

The results of the two experiments are only apparently contradictory. Actually, they are not, because they point out that either one (e.g. intra-die) or the other (inter-die) effects (or both) may affect the performance of the clock tree. Therefore, the design of a clock distribution network should take into account all the possible causes of performance degradation, including, in particular inter and intra-die process variation. They have also shown that the mismatch can also be of concern for digital designs.

## Acknowledgments

The authors are grateful to R. Burger, P. Delpech and P. Llinares of STMicroelectronics for providing the design of the Viterbi encoder and the process characterization data, to T. Lin and N. Dragone of Carnegie Mellon University for the help on physical clock tree routing and for the many useful discussions and to P. McNamara of PDF Solution Inc. for the help on the GPU simulations.

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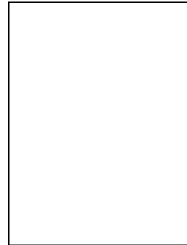

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