Accelerated 65nm Yield Ramp through Optimization of Inspection on Process-Design Sensitive Test Chips

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Abstract

This paper describes an integrated methodology that combines short-flow test chips useful for exploring process-design systematic as well as random failure modes and an advanced inspection tool platform to characterize and monitor key Defects-of-Interest for accelerated defect-based yield learning at the 65nm technology node. Utilization of a unique fast electrical testing scheme, rapid analysis software along with optimized inspection facilitated shorter learning cycles for accelerated process development. Knowledge derived from the CV®-based inspection setup in a leading 300mm fab was successfully transferred to manufacturing to facilitate inspection optimization for key Defects-of-Interest *on product wafers.*

Keywords: Characterization Vehicle®, CV®, Test chips, Defect Inspection, Defect Overlay Analysis, S/N analysis, KLA-Tencor, 2800, Process-Design interactions

I. Introduction

The emergence of highly complex system-on-a-chip (SOC) technologies has provided unique challenges to yield learning during product yield ramp. In particular, rapid detection of process-design based yield limiters is complicated by ever increasing design complexity which makes it difficult to capture and localize yield relevant killer defects or Defects-of-Interest directly on product. To address these issues and rapidly characterize the impact of process changes on DOIs during the yield ramp, the authors propose an integrated inspection methodology which combines the use of PDF Solution's innovative short-flow Characterization Vehicle® (CV®) test chips along with KLA-Tencor's BrightField Inspection System and inspection optimization strategies.

This work employed KLA-Tencor's best-of-breed 2800 series wafer inspection tool, which provides a Deep UV Broadband Inspection System with multiple wavelengths to ensure maximum sensitivity for defect detection. In addition, KLA-Tencor's In-line Defect Organizer (iDO) aided the defect characterization process in that it provided an effective defect binning capability to quickly identify yield limiting defects-of-interest. The following sections will describe the elements of the integrated methodology in more detail.

II. Short-Flow Characterization Vehicle® (CV®) Test Chips

PDF Solution's short-flow Characterization Vehicle® (CV®) test chips provide a powerful, comprehensive platform for identifying both systematic and random defect-based yield limiters [1]. The diverse layout patterns of the CV® test chips allow for the rapid detection of product-style issues. They also provide an improved inspection platform for defect-based yield learning compared to product, where defects can be more difficult to localize. PDF CV® test chips provide typically greatly increased or comparable defect critical area across all front-end-of-line (FEOL) and back-end-of-line (BEOL) module layers. This enables accurate estimation of electrical defect contact/via fail rate (λ) and defect density (D0) for process split lot assessment or product-based yield impact modeling using PDF's product-based yield impact table (YIMP) methodology

[2]. CV® test chips also provide a significantly reduced test time which is achieved by electrically testing the CV® test chips in the fab using a dedicated massively parallel tester (pdFasTest®). This testing system is 10-15x faster than current parametric test systems [3]. Once both the inline inspection and electrical data from the CV® test chips are loaded into the pdCV™ software analysis environment, the engineer can rapidly perform the following analyses: 1) inline defect overlay analysis to electrical data for defect kill ratio/capture rate (KR/CR) analysis, 2) yield modeling or fail rate analysis as a function of CV® structure design attributes, and 3) extraction of candidate electrical fail sites for inline dual-beam FIB and/or physical failure analysis [3]. These benefits along with the inline defect inspection tool enable a faster manufacturing yield ramp by providing an infrastructure to rapidly characterize and monitor the impact of process fixes on key DOI in the overall defect Pareto.

III. Defect Inspection System and Methodology

The 2800 inspection system uses a time delay integration (TDI) sensor to detect the reflected light image of the defects as the wafer scans below the sensor, making the system very sensitive to all defects. The inspection tool is an image comparison tool that compares a reference to a candidate region and identifies the defective pixels in that region. The TDI sensor amplifies the reflected signal, converting the optical image into a digital pixelized image, or patch image which is then sent to the image computers.

The 2800 in-line wafer inspection tool has multiple optical and spectral mode capabilities for more rapid recipe optimization allowing for efficient defect inspections based on defect sensitivity. The tool uses an ultra-broad band (UBB) light source where multiple Deep UV, UV, and visible wavelengths can be used interchangeably. To determine the proper inspection mode and inspection pixel size it is important to have some knowledge of the design rules and process specifications. The inspection pixel size directly influences the sensitivity of the recipe, the spectral modes available, and the inspection throughput.

One of the more important parts of recipe setup is the care area selection which ultimately establishes what areas of the chip will be concentrated on for the detection and characterization of key DOI for yield improvement. These areas on the CV® test chips include an extensive set of experiments employing Nest and Snake & Comb test structures (as shown in Fig 1) across multiple design rules and pattern densities to capture defects causing electrical opens or shorts via defect overlay analysis. The nest structure also allows for characterization of the defect size distribution [4].

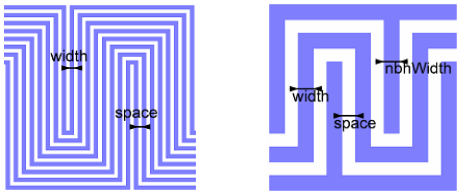

Fig.1: Examples of the Nest (left) and Snake & Comb (right) test structures from the PDF CV® test chip used for detect detection and characterization via electrical overlay analysis.

Moreover, these critical inspection areas or care areas on the CV® test chips are grouped into separate regions based on current layer density and split by the underlying layer density. The optical inspection recipe for each region is individually optimized to provide the best optical sensitivity especially to help capture potentially pattern-dependent key DOI during CV® wafer inspection.

After the initial setup sensitivity optimization is completed just to create a wafer map with a manageable amount of defects detected. Next the defects are reviewed on the eDR 5000 SEM review tool.

Recipe optimization continues back on the inspection tool once several level critical defects have been identified, which is as significant as additionally identifying non-critical or nuisance defects. The initially inspected wafer is loaded back on the inspection tool for a signal-to-noise (S/N) analysis. The S/N analysis is the focal point of the recipe optimization and it allows the defect locations to be individually characterized for comparison of several optical and spectral modes at one time. Not only is it important to decide on a mode that has a strong signal to the critical defects but it is moreover hugely valuable to choose a mode that best suppresses the nuisance type defects or has a low S/N value, thus making the inspection that much more efficient at detecting mostly killer defects.

Once the optimum optics mode has been selected it is important to then implement that mode into the inspection recipe, make a few adjustments to the recipe sensitivity, scan and

SEM review another wafer. One advantageous feature provided by the KLA-Tencor SEM review tool is the ability to tune the threshold or sensitivity values of an inspection recipe during review, supplying immediate feedback on the wafer map and defect counts.

The last recipe optimization technique used during this accelerated yield learning project was KLA-Tencor's in-line defect organizer. Using iDO allows the user to arrange the detected defects into bins and supports the concepts of smart SEM review sampling, nuisance filtering, and SPC charting. Automatic defect classification (ADC) and rules based binning (RBB) form the backbone of iDO. Both techniques, ADC and RBB, are computer based in-line image processing methods used to automatically and rapidly sort different defect types into appropriate bins and it is more accurate, consistent, economical, and faster than manually classifying.

ADC is based on the small image patches from the inspection tool, including both the defect and background information from the patch. Each patch is described using a series of feature vectors where a feature vector is a quantifiable attribute defining a defect image. The ADC classifier works by comparing the feature vectors of newly detected defects to those of saved images and the newly detected defects are assigned a bin that it most closely resembles.

Unlike ADC, which requires some minor optimization, RBB is more robust as it is based not so much on the feature vectors determined from the patch images, but from the defect attributes. Upon detection each defect is defined with attributes such as size and polarity making rules-based binning of defects possible.

iDO is represented by a tree structure diagram, similar to the iDO tree shown in Fig. 2. A typical iDO tree consists of a few RBB attributes to separate nuisance or noise defects and then a subsequent ADC classifier to separate real defect types into different bins, but it could also be built in the opposing order. Once the iDO tree classifier is built and proven the bins are labeled with a defect class code allowing for quick and accurate identification of killer and non-killer defects. SEM smart sampling can be done based on the iDO class codes, by sampling a greater percentage of defects from the DOI bins.

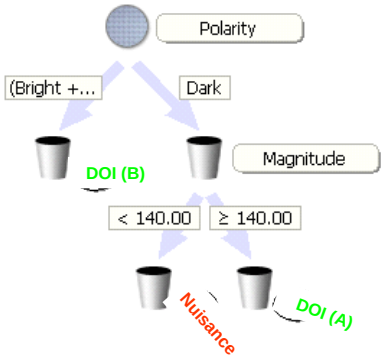

Fig.2: Example iDO Tree

Once recipe setup and optimization has been completed ensuring maximum defect detection sensitivity with the most efficient optical and spectral settings, then it is up to manufacturing to manage the processing and testing of the short-flow test chip CV® wafers to enable defect overlay analysis and the characterization of key DOI.

IV. Characterization of Key Defects-of-Interest

One important contribution of this integrated methodology was to help monitor and characterize key FEOL and BEOL DOI on the yield ramp's defect Pareto and help assess the impact of process changes directed at reducing those DOI. Examples of key DOI include: Hollow Metal (HM) (Fig 3), Box Divots (Fig 4), Missing Ni silicide (Fig 5), and CMP polish scratches.

The hollow metal (HM) defect was a key BEOL DOI on the defect Pareto causing metal opens. To speed up the learning, the BEOL CV® was deployed especially since it runs just a portion of the process flow, needing only a single metal level for this HM defect mode. Subsequently, the BEOL CV® could be run at ~2-3x faster cycle time than product lots, thus accelerating the learning. In addition, because the care areas could be chosen carefully based on the current and underlying density, the inspection was more easily optimized on the CV® test chip vs. on product.

The hollow metal defect mechanism provided a special challenge to inspection recipe setup and tuning given the high defect nuisance rate introduced by this defect, so special care was given to inspection recipe optimization. In addition to using specific care areas based on the CV® test chip design, different tools were used

to help optimize the recipes including feedback from electrical defect overlay analysis. Table 1 shows the improvement afforded in terms of defect overlay capture rates (CR) and electrical kill ratios (KR) by the initial optimized CV®-based 2800 inspection setup at M3 compared to the previous inspection setup using an older-generation brightfield inspection tool. Moreover, Fig. 6 illustrates the improvement afforded by the 2800 over the 2351 in capturing more of the single-line M3 open electrical fails typically caused by small flake missing pattern (MP) defects.

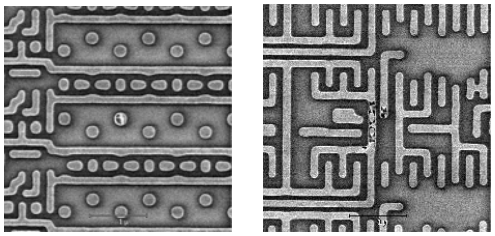

Fig.3: Examples of the Hollow Metal defect.

CV-based M3 BF Inspection Comparison	Opens KR	Opens CR	Shorts KR	Shorts CR
Delta Improvement	+19%	+14%	-2%	+35%

Table 1: Initial CV®-based inspection sensitivity improvement at M3 BEOL inspection level for the 2800 inspection system compared to the previous inspection setup using the 2351.

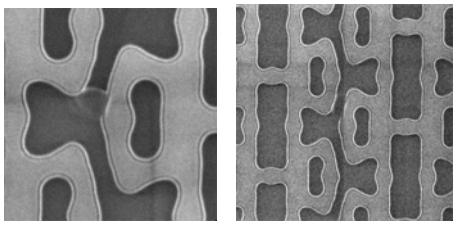

Fig.4: Examples of the Box Divot defect.

At the active (Rx) inspection level where the box divot defect was an especially key DOI, the 2800-based inspection enabled improvement in active (Rx) hard shorts CR by 13-15% compared to the 2351 system. Additionally, the 2800 showed a 4-5% CR improvement vs. the 2351 for CMP polish scratches and box divot defects causing active level soft shorts. Finally, Fig. 7 shows the improved defect capture rate at the NiSi inspection level using the 2800 integrated inspection methodology for various defect types contributing to poly hard open electrical fails.

V. Transfer of CV®-based Inspection Mode Learning to Product Inspection

Another important contribution was the ability to transfer the Best-Known-Method (BKM) developed from the PDF CV®-based 2800 inspection mode setup and optimization work to build the inspection recipes on product wafers right from the start of the production ramp. By using the Optics Selector feature in 2800 inspector, the best inspection mode could be determined based on the defect's signal-to-noise (S/N) ratio as measured by the inspector.

Examples of two DOI where such an optimized inspection mode transfer to manufacturing took place include the Box Divot defect (Fig. 4) and Missing Ni Silicide defect (Fig. 5). In both cases, inspection mode learning derived first on CV® test chips enabled more accurate and reliable detection on product than had been achieved previously. Also, defect examples were quickly identified on the CV® test chips using feedback from electrical test via overlay analysis. This gave guidance to the inspection engineer as to the defect to focus on for recipe optimization. Due to a well-controlled layout on the CV®, the inspection recipe could be optimized given specific care areas with constant density regions. Using the Poly CV® for the process learning combined with the optimized inspection, the learning cycle was shortened by ~2-3x compared to the learning on product.

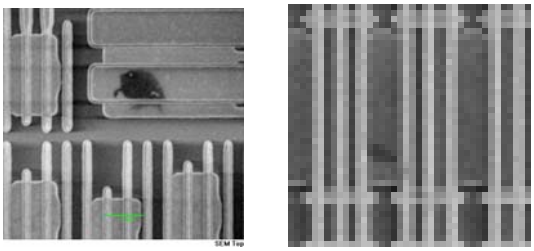

Fig.5: Example of Missing Ni Silicide Defect on product (left) and PDF CV® test chip (right)

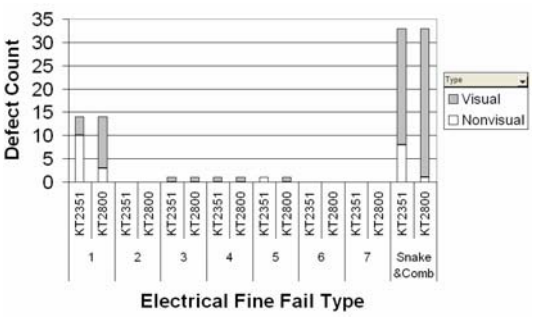

Fig. 6: Electrical fail Pareto illustrating the improved capture of inline defects causing single-line M3 open electrical fails by the 2800 vs. the 2351 as a function of Nest and Snake & Comb test structure fine fail type (# of test structure lines electrically open). (Note: Visual = inline defect overlay detected for corresponding electrical open. Nonvisual = no inline defect found for corresponding electrical open fail, e.g., a buried or prior-level defect)

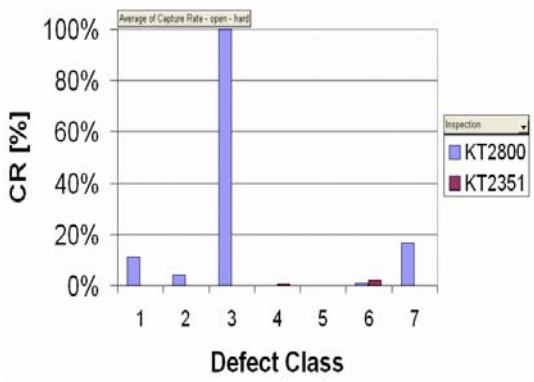

Fig. 7: Chart illustrating the improved CR afforded by the 2800 vs. the 2351 for several defect classes at the NiSi inspection level contributing to poly hard open electrical fails.

VI. Conclusion

This paper presented an integrated inspection methodology that combined the use of short-flow Characterization Vehicle® (CV®) test chips that can explore process-design systematic as well as random fail modes and an advanced inline defect inspection tool platform to characterize and monitor key Defects-of-Interest from the yield ramp defect Pareto.

PDF's CV® test chips enabled significant yield learning cycle time improvement (~2-3x vs. product cycle times) for IBM, especially by helping to characterize and address process-design systematic marginalities earlier in the yield ramp. By using PDF's CV® test chips along with the 2800 inspection tool platform, IBM was able to quickly and effectively characterize key DOI on the yield ramp defect Pareto as well as characterize the defect-based yield improvement afforded by new process changes targeted at those key DOI.

The integrated methodology provided the following advantages for IBM: 1) increased detection of CMP polish scratches with the 2800 vs. the 2351 inspection system, 2) improved capture of the NiSi inspection level missing silicide DOI with inspection learning transferred to product, 3) identification of the box divot DOI not initially detected on product, and 4) effective characterization of the impact of the Front-Side SEZ clean and 4 step liner process on the hollow metal DOI.

Finally, inspection mode learning derived from the CV®-based 2800 inspection mode setup and optimization for several key DOI on the defect Pareto, e.g., the box divot and missing silicide DOIs, was successfully transferred to manufacturing to facilitate DOI inspection characterization and monitoring on product wafers.

VII. Acknowledgments

The authors would like to acknowledge Anne Murray, Sherry Lee, Gary Crispo, Sa Zhao, Steve Poon, Zach Berndlmaier, Brian Duffy, Malcolm McLean, and Sumanth Kini for their helpful suggestions and support with this collaborative work.

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